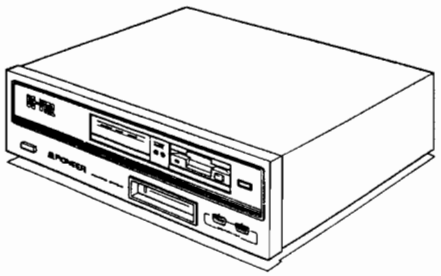
PIONEER®

Service Manual

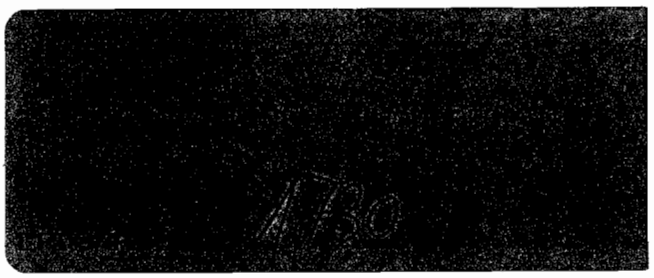


ORDER NO.
ARP1290-A

CIRCUIT DESCRIPTIONS
REPAIR & ADJUSTMENTS

VIDEO DISC CONTROLLER

UC-V102



- **This service manual is applicable to the KUC type .**

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1730

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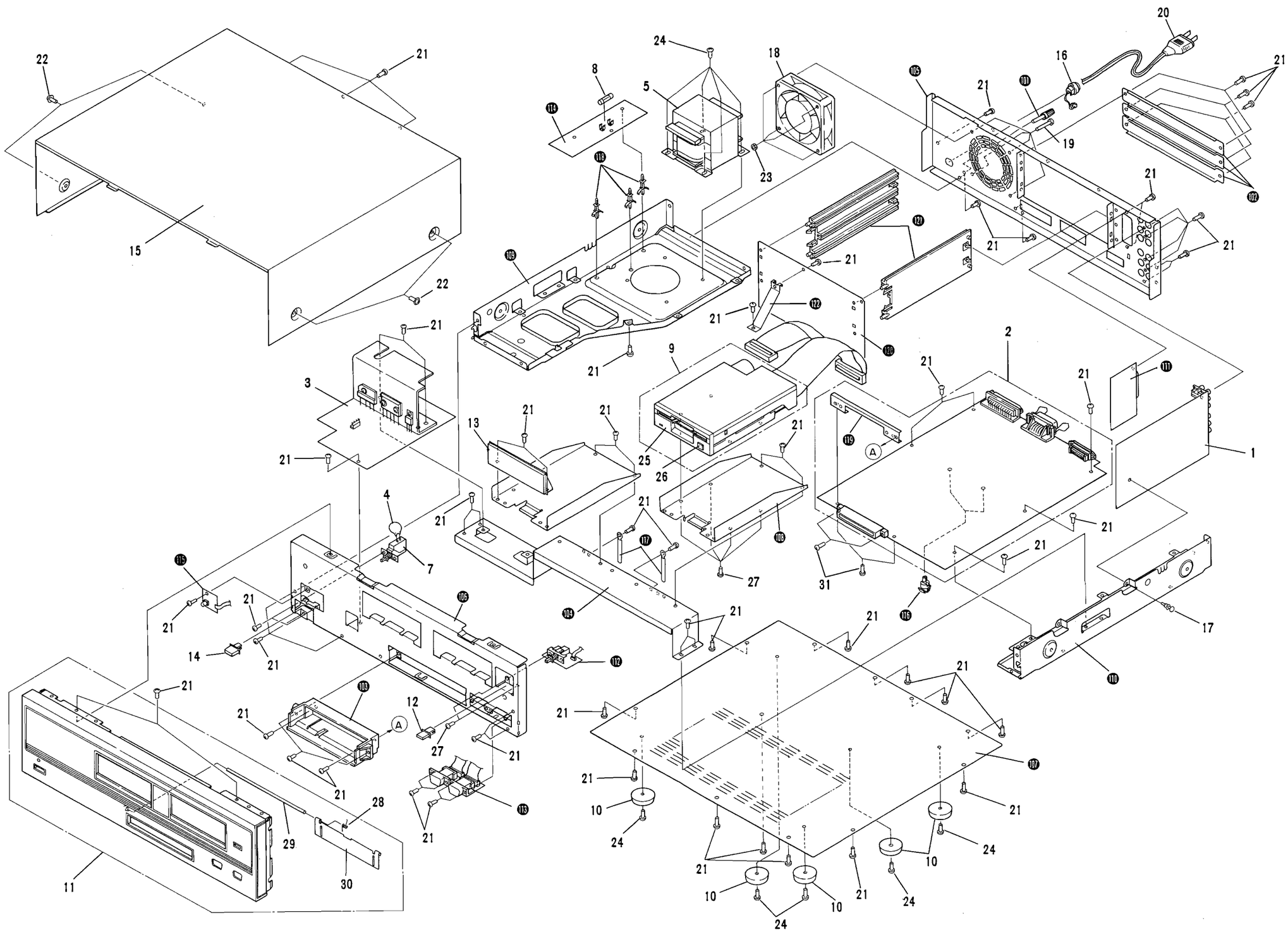
1. EXPLODED VIEW AND PARTS LIST

NOTES:

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

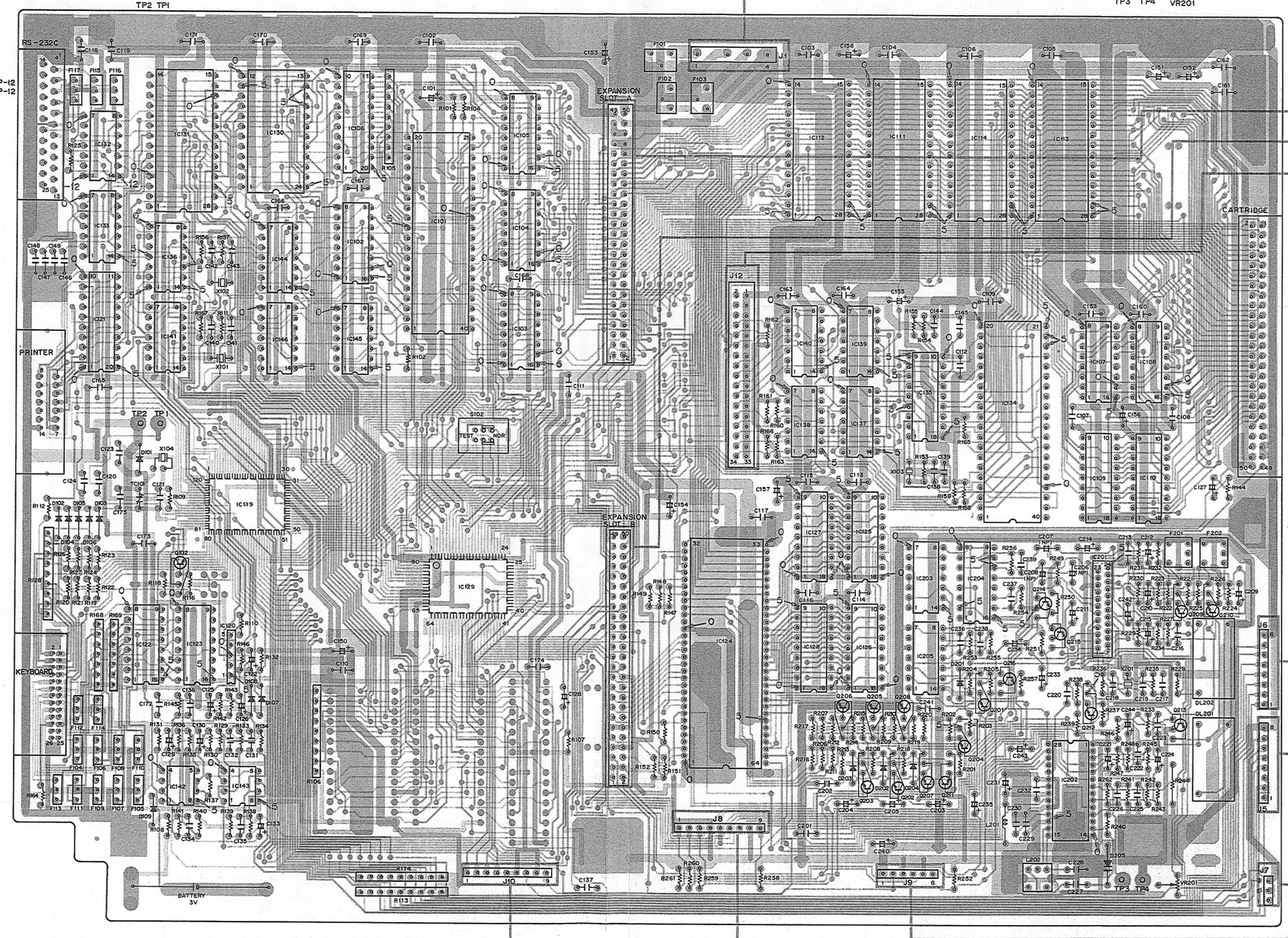
Parts List

Mark	No.	Part No.	Description
	1	AWZ1172	AV SW assembly
	2	AWZ1186	CPU assembly
	3	AWZ1177	Regulator assembly
⚠	4	ACG1003	Capacitor (0.01/AC125V,C1,C2)
⚠ ★	5	ATT1030	Power transformer (T1)
⚠★★	7	ASG-546	Push switch (POWER,S1)
⚠★★	8	AEK-121	Fuse (1.6A,FU1)
	9	AXX1004	Floppy disc drive (FLOPPY A)
	10	AEC-613	Foot assembly
	11	ANB1059	Front panel assembly
	12	AAD1083	Push knob A (RESET)
	13	AAK1145	Disc cover
	14	AAY-304	Push knob B (POWER)
	15	ANE1054	Bonnet case
⚠	16	AEC1026	AC cord stopper
	17	AEC-441	Nylon rivet
★★	18	AXM1004	Fan motor
	19	ABA1013	Screw (M4×35)
⚠	20	ADG1007	AC power cord
	21	BBZ30P080FZK	Screw
	22	FBT40P080FZK	Screw
	23	NA40FMC	Nut (M4)
	24	VBZ40P080FMC	Screw
	25	AZN1210	Panel
	26	AZA1043	Button
	27	VMZ30P060FMC	Screw
	28	ABH-168	Door spring
	29	ABH-034	Door shaft
	30	AAH1011	Cartridge door
	31	BBZ30P100FZK	Screw
	101		Terminal (GND)
	102		Rear cover
	103		Cartridge holder (F)
	104		F.D. support flame
	105		Rear panel
	106		Panel stay
	107		Bottom plate
	108		F.D. holder
	109		Transformer flame
	110		Right flame
	111		RGB assembly
	112		SW assembly
	113		Connector assembly (1)
	114		Filter assembly
	115		LED assembly
	116		PCB holder
	117		Binder
	118		PCB support
	119		CN angle
	120		Connector assembly (2)
	121		Guide rail
	122		Connector holder


1
2
3
4
5
6
A
B
C
D
22
21
15
24
8
5
18
20
16
114
23
105
101
19
102
109
121
122
9
2
13
25
26
111
119
1
4
7
27
31
116
17
115
14
112
103
12
110
28
29
30
11
10
107
24

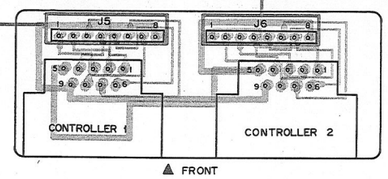
2. P. C. BOARDS DIAGRAM

CPU ASSEMBLY (AWZ1186)

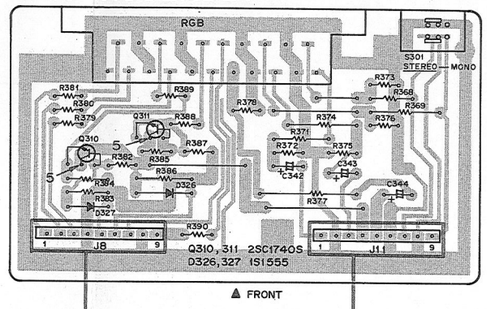


IC101	LH0080A
IC102~105	M74LS367AP
IC106	M74LS245P
IC107,108	M74LS157P
IC109,110,125~128	MB81464-12 or TMM4464P-12 or M5M4464P-12
IC111	M5L27256K-MM
IC112	M5L27128K-ME
IC113	M5L27128K-FD
IC114	M5L2764K-RS
IC119	S1985
IC120	M51954BL
IC121	M74LS373P
IC122,123	M74LS156P
IC124	V9938C
IC129	PD5044
IC130	M5L8253P-5
IC131	M5L8251AP-5
IC132	M75188P
IC133	M75189AP
IC134	M5W1793-02P
IC135	SED9421C0B
IC136	M74LS74AP
IC137,205	M74LS04P
IC138	M74LS14P
IC139,140	M74LS38P
IC141	TC74HCU04P
IC142,143	M5218P
IC144	M74LS08P
IC145	M74LS30P
IC146	M74LS32P
IC201	BA7230LS
IC202	V7010
IC203	M74LS00P
IC204	M74LS123P
Q102,201,205,205, Q208,213,215	2SA933S
Q202~204,207,209, Q210,212,214	2SC1740LS
Q211,216	DTC124ES
D101~109,201~204	1S1555
D205	ITT310

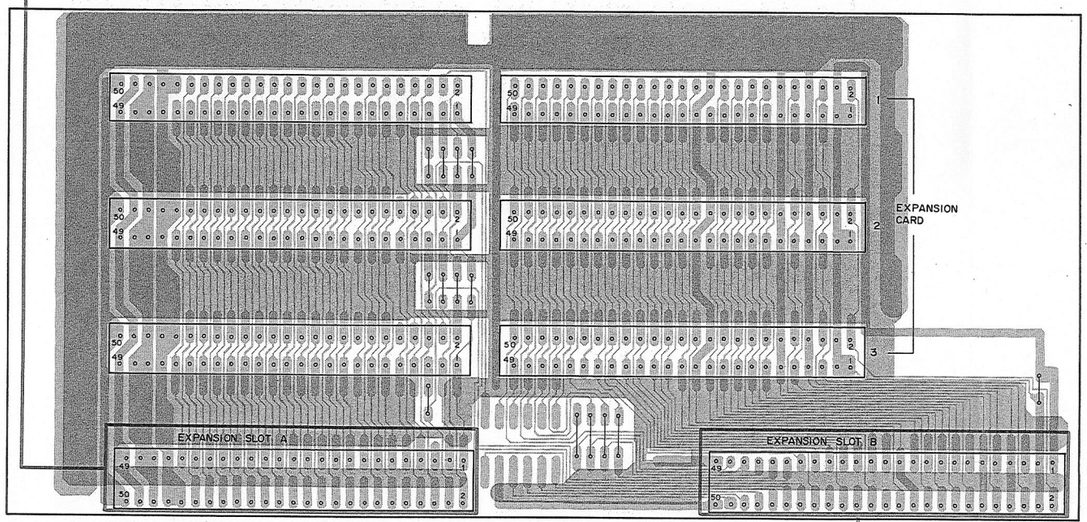
CONNECTOR ASSEMBLY (1)



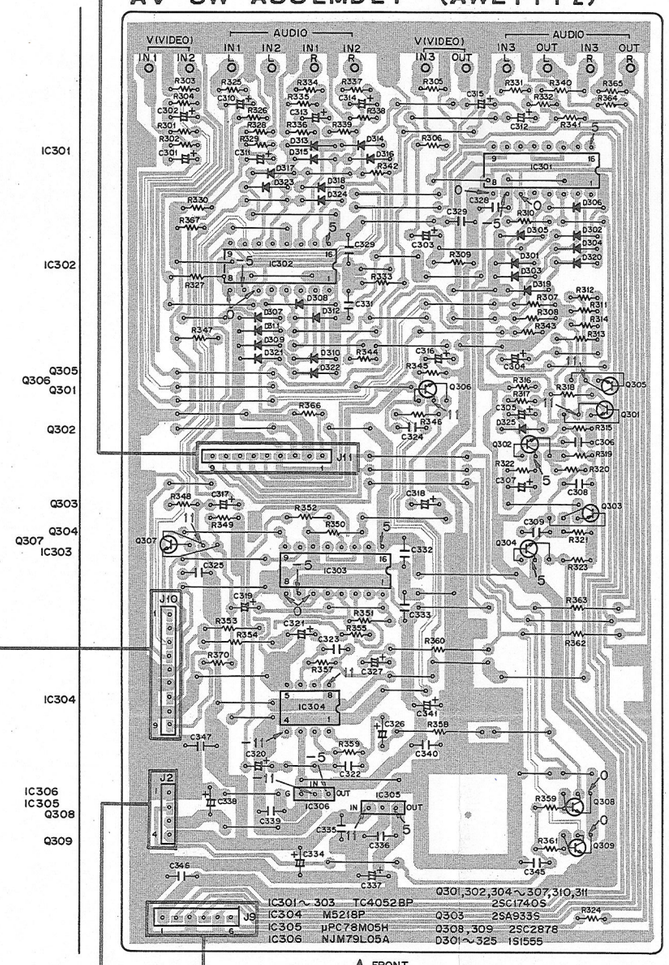
RGB ASSEMBLY



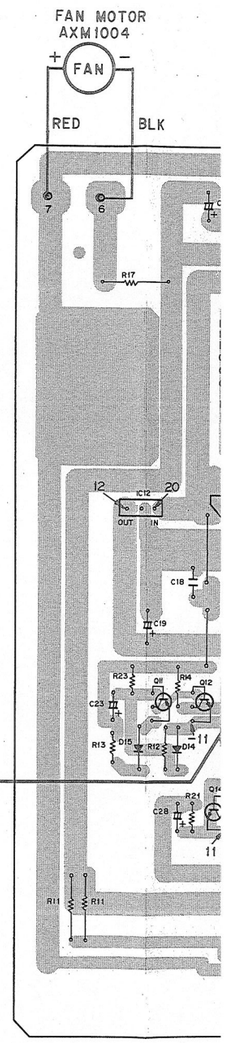
CONNECTOR ASSEMBLY (2)

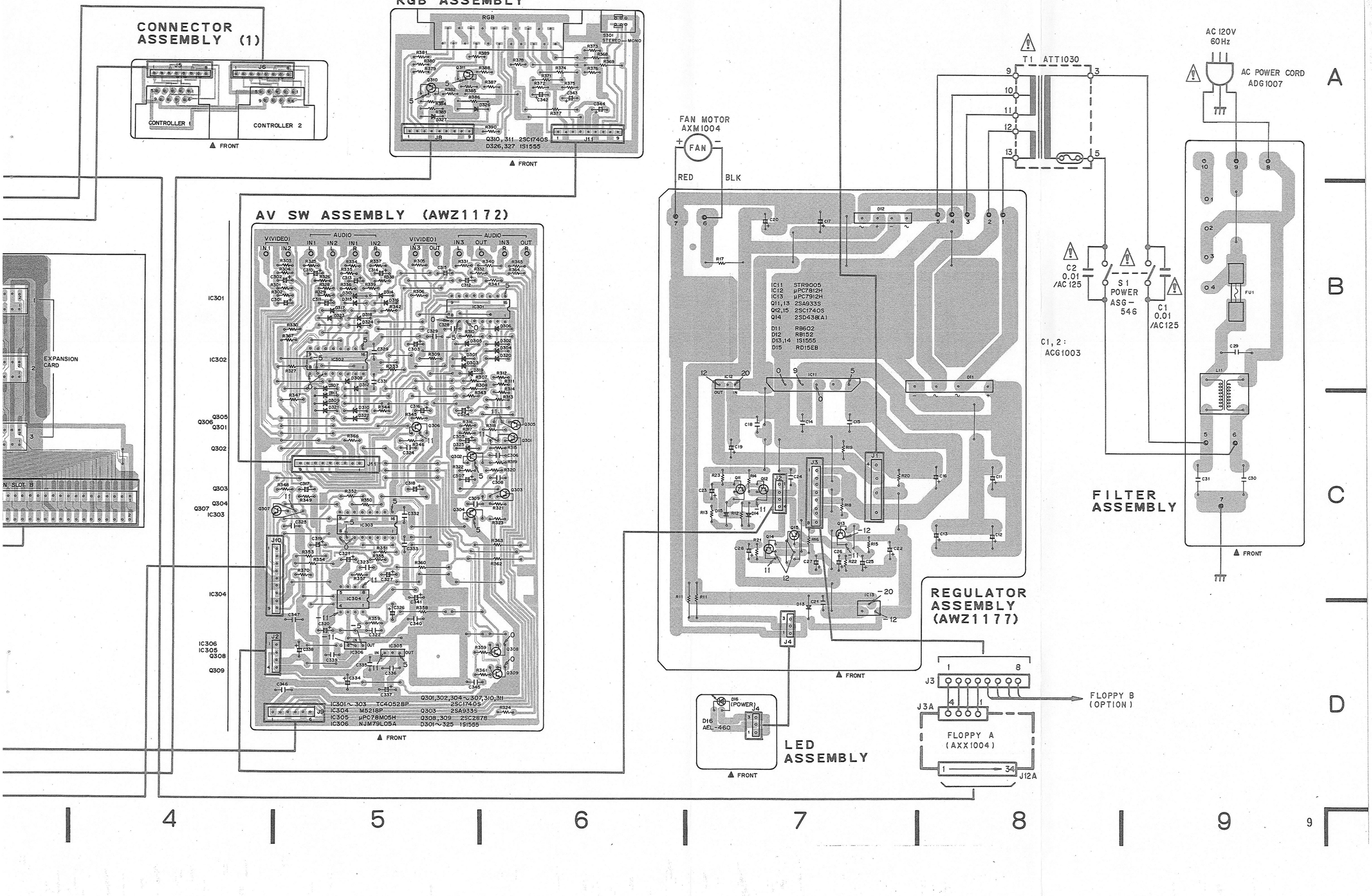


AV SW ASSEMBLY (AWZ1172)

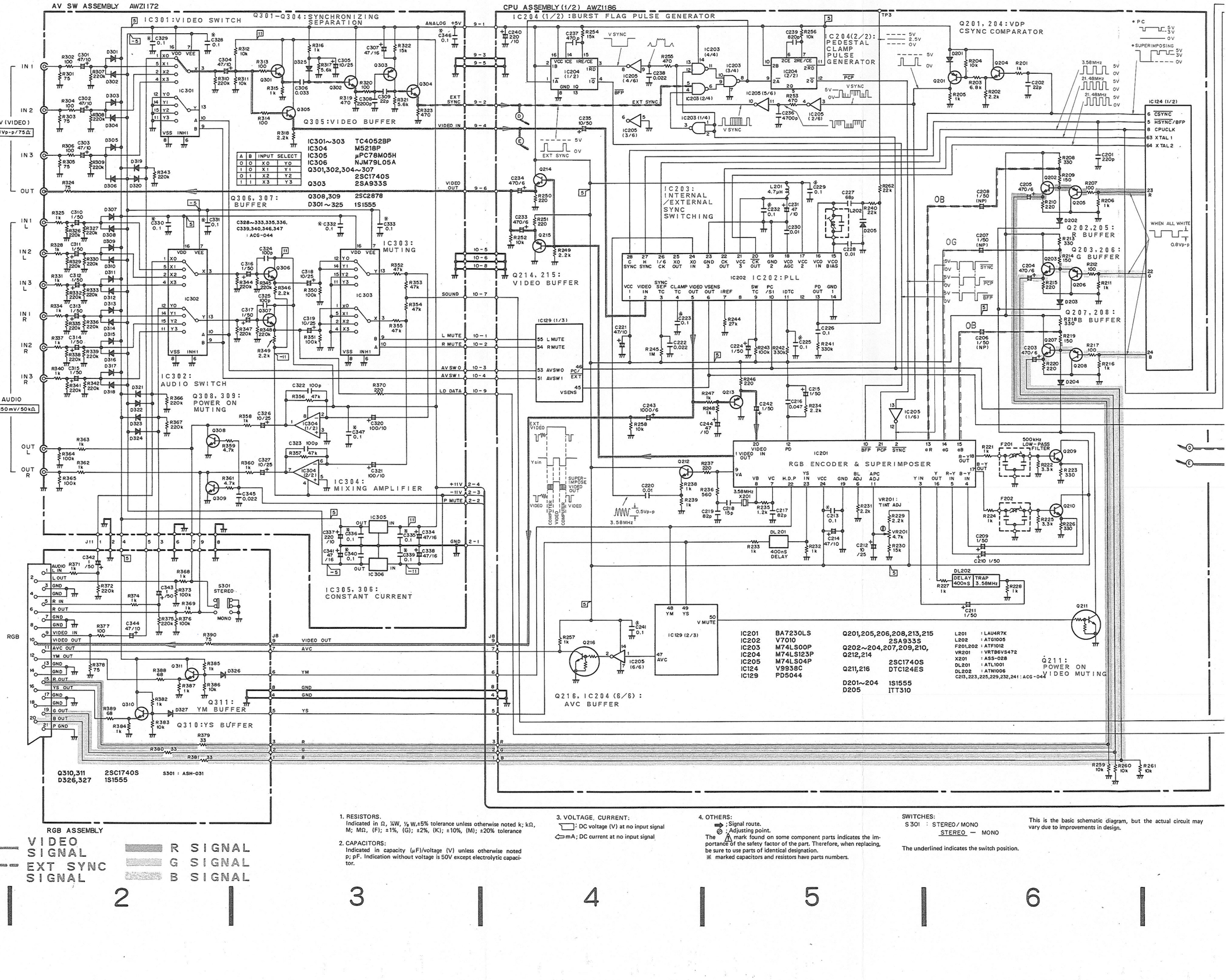


FAN MOTOR AXM1004




CONNECTOR ASSEMBLY (1)
J5
J6
CONTROLLER 1
CONTROLLER 2
FRONT
RGB ASSEMBLY
RGB
S301 STEREO — MONO
J8
J11
Q310, 311 2SC1740S
D326, 327 1S1555
FRONT
AV SW ASSEMBLY (AWZ1172)
V(VIDEO) IN1
IN2
AUDIO IN1 L
IN1 R
IN2 L
IN2 R
V(VIDEO) IN3
OUT
AUDIO IN3 OUT L
IN3 OUT R
IC301
IC302
Q305
Q306
Q301
Q302
Q303
Q304
Q307
IC303
IC304
IC306
IC305
Q308
Q309
J11
J10
J2
J9
IC301~303 TC4052BP
IC304 M5218P
IC305 μPC78M05H
IC306 NJM79L05A
Q303 2SA933S
Q308, 309 2SC2878
D301~325 1S1555
Q301, 302, 304~307, 310, 311 2SC1740S
FRONT
EXPANSION CARD
SLOT B
FAN MOTOR AXM1004
FAN
RED
BLK
IC11 STR9005
IC12 μPC7812H
IC13 μPC7912H
Q11, 13 2SA933S
Q12, 15 2SC1740S
Q14 2SD438(A)
D11 RB602
D12 RB152
D13, 14 1S1555
D15 RD15EB
J1
J2
J3
J4
REGULATOR ASSEMBLY (AWZ1177)
FRONT
D16 (POWER)
D16 AEL-460
LED ASSEMBLY
FRONT
T1 ATT1030
AC 120V 60Hz
AC POWER CORD ADG1007
C2 0.01 /AC125
S1 POWER ASG-546
C1 0.01 /AC125
C1, 2: ACG1003
FU1
FILTER ASSEMBLY
FRONT
J3
J3A
FLOPPY B (OPTION)
FLOPPY A (AXX1004)
J12A

3. SCHEMATIC DIAGRAM



1. RESISTORS.
Indicated in Ω, ¼W, ⅓ W,±5% tolerance unless otherwise noted k; kΩ, M; MΩ, (F); ±1%, (G); ±2%, (K); ±10%, (M); ±20% tolerance

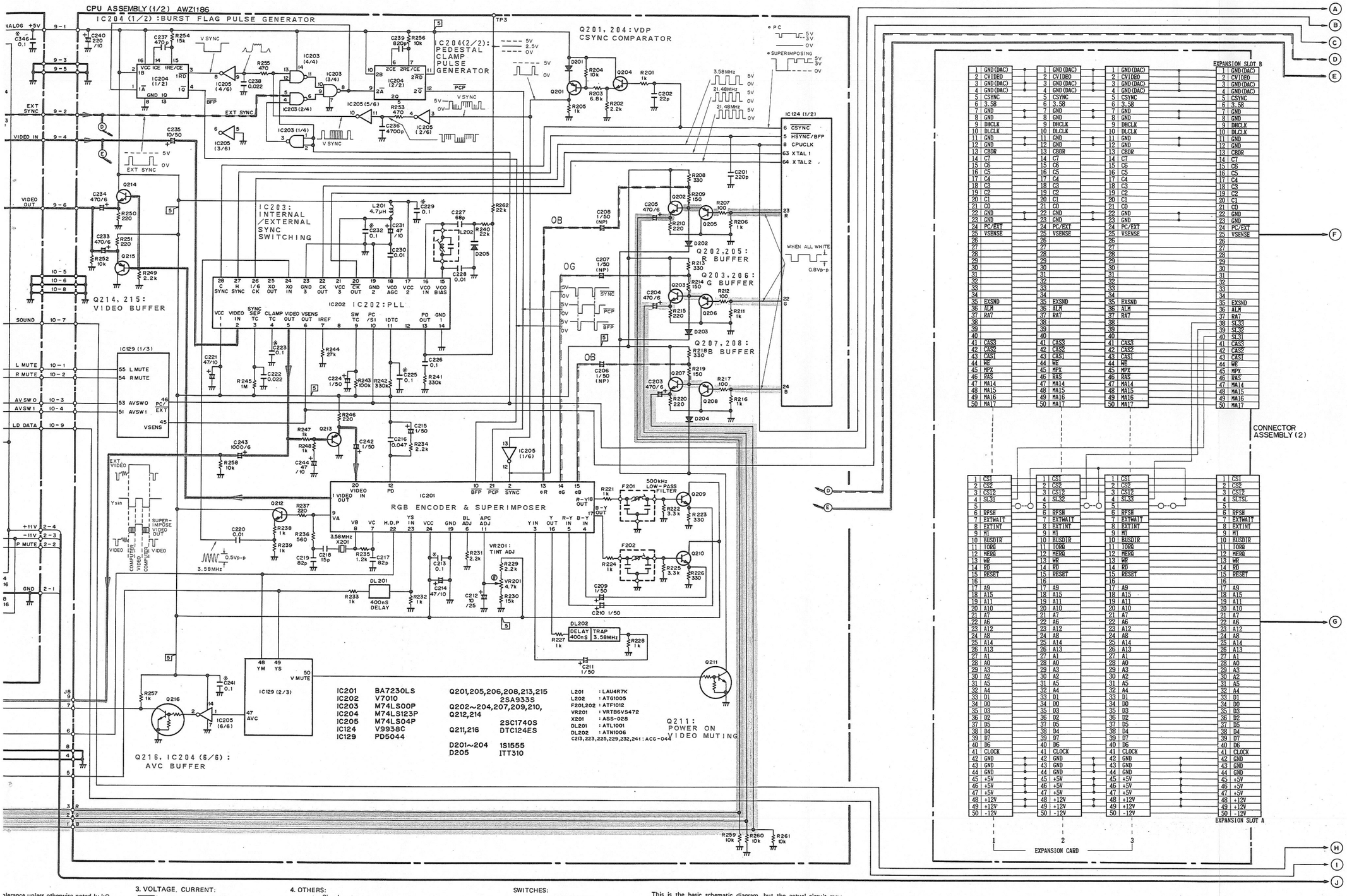
2. CAPACITORS:
Indicated in capacity (μF)/voltage (V) unless otherwise noted p; pF. Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT:
▭: DC voltage (V) at no input signal
⇦mA; DC current at no input signal

4. OTHERS:
⇨; Signal route.
⊘; Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
※ marked capacitors and resistors have parts numbers.

SWITCHES:
S301 : STEREO / MONO
STEREO — MONO
The underlined indicates the switch position.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.



3. VOLTAGE, CURRENT:
□: DC voltage (V) at no input signal
⇦ mA; DC current at no input signal

4. OTHERS:
➡ ; Signal route.
⊘ ; Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
※ marked capacitors and resistors have parts numbers.

SWITCHES:
S301 : STEREO / MONO
STEREO — MONO
The underlined indicates the switch position.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

CPU ASSEMBLY (2/2) AWZ1186

EXT SYNC SIGNAL

VIDEO SIGNAL

EXPANSION SLOT B

1	GND(DAC)
2	CVIDEO
3	GND(DAC)
4	GND(DAC)
5	CSYNC
6	3.58MHz
7	GND
8	GND
9	DHCLK
10	DLCLK
11	GND
12	GND
13	CBDR
14	C7
15	C6
16	C5
17	C4
18	C3
19	C2
20	C1
21	C0
22	GND
23	GND
24	PC/EXT
25	VSENSE
26	NC
27	NC
28	NC
29	NC
30	NC
31	NC
32	NC
33	NC
34	NC
35	EXSND
36	ALM
37	RA7
38	SL33
39	SL32
40	SL31
41	CAS3
42	CAS2
43	CAS1
44	WE
45	MPX
46	RAS
47	MA14
48	MA15
49	MA16
50	MA17

EXPANSION SLOT A

1	CS1
2	CS2
3	CS12
4	SLTSL
5	NC
6	RFSH
7	EXTWAIT
8	EXTINT
9	M1
10	BUSDIR
11	IORQ
12	MERQ
13	WR
14	RD
15	RESET
16	NC
17	A9
18	A15
19	A11
20	A10
21	A7
22	A6
23	A12
24	A8
25	A14
26	A13
27	A1
28	A0
29	A3
30	A2
31	A5
32	A4
33	D1
34	D0
35	D3
36	D2
37	D5
38	D4
39	D7
40	D6
41	CLOCK
42	GND
43	GND
44	GND
45	+5V
46	+5V
47	+5V
48	+12V
49	+12V
50	−12V

CARTRIDGE SLOT

1	CS1
2	CS2
3	CS12
4	RFSH
5	NC
6	EXTWAIT
7	EXTINT
8	M1
9	BUSDIR
10	IORQ
11	MERQ
12	WR
13	RD
14	RESET
15	NC
16	A9
17	A15
18	A11
19	A10
20	A7
21	A6
22	A12
23	A8
24	A14
25	A13
26	A1
27	A0
28	A3
29	A2
30	A5
31	A4
32	D1
33	D0
34	D3
35	D2
36	D5
37	D4
38	D7
39	D6
40	GND
41	CLOCK
42	GND
43	GND
44	SW1
45	+5V
46	SW2
47	+5V
48	+12V
49	SNDIN
50	−12V

IC101: CPU

IC102(1/3), IC103, IC104: ADDRESS BUS BUFFER

IC144 (2/4): INTERRUPT CIRCUIT

IC141 (4/6, 5/6), IC102 (2/3): CPU CLOCK GENERATOR

X101: 3.579545MHz

IC107, IC108: RAM ADDRESS MULTIPLEXER

IC106: DATA BUS BUFFER

IC105: CONTROL BUS BUFFER

IC109, IC110: MAIN RAM

IC111: MSX BASIC ROM

IC112: MSX EXTENSION BASIC ROM

IC113: DISC BASIC ROM

IC114: RS-232C ROM

IC146(2/4, 3/4): EXTENSION BASIC ROM CHIP SELECT

IC145: RSEL GENERATOR

IC146(1/4): BASIC ROM CHIP SELECT

IC124 (2/2), IC125~IC128: VIDEO PROCESSING CIRCUIT

IC124 (2/2): VDP

IC125, IC127: V-RAM

IC120: RESET

IC121: PRINTER INTERFACE

IC141 (3/6): RESET SIGNAL INVERTER

IC102 (3/3): PSTB BUFFER

IC119: MSX-SYSTEMII

IC136 (1/2), IC144 (1/4): PPI SOUND CONTROL

IC142 (2/2), IC143: CPE DATA READER

Q102: CAPS LED DRIVER

IC101	LH0080A	IC119	S1985	IC137
		IC120	M51954BL	IC138
		IC121	M74LS373P	IC139,140
				IC141
				IC142,143
IC102~105	M74LS367AP	IC122,123	M74LS156P	IC144
IC106	M74LS245P	IC124	V9338C	IC145
IC107,108	M74LS157P	IC129	PD5044	IC146
IC109,110,125~128	MB81464-12 or	IC130	M5L8253P-5	
M5M4464P-12 or	TMM41464P-12	IC131	M5L8251AP-5	
IC111	M5L27256K-MM	IC132	M75188P	Q102
IC112	M5L27128K-ME	IC133	M75189AP	D101~109
IC113	M5L27128K-FD	IC134	M5W1793-02P	
IC114	M5L2764K-RS	IC135	SED9421C0B	
		IC136	M74LS74AP	

DATA BUS
ADDRESS BUS
CONTROL I
CONTROL II

), IC125~IC128:
CESSING CIRCUIT

IC129:GATE ARRAY

IC130~IC133:
RS-232C
INTERFACE

IC125 V-RAM
IC126 V-RAM
IC127 V-RAM
IC128 V-RAM

IC129 (3/3)

IC130 PIT

IC131 USART

RS-232C

OPTION

FLOPPY A (AXX1004)
FLOPPY B (AXX1004)

FILTER ASSEMBLY
C29 : ACG1002
C30,31 : ACG-505
L11 : ATF-168
FU1 : AEK-121
C1, 2 : ACG1003
S1 POWER ASG-546
AC 120V 60Hz
AC POWER CORD ADG1007

REGULATOR ASSEMBLY AWZ1177
IC11~IC13: REGULATOR

Q13~15: REGULATOR

Q11, 12: POWER MUTING

FAN MOTOR AXM1004

D16 (POWER)
LED ASSEMBLY

IC11	STR9005	Q12,15	2SC1740S
IC12	μPC7812H	Q14	2SD438(A)
IC13	μPC7912H	Q11	RBV602
Q11,13	2SA933S	D11	RB152
D13,14	1S1555	D15	RD15EB

C11~13 : ACH-382

IC137	M74LS04P		
IC138	M74LS14P		
C119	S1985	IC139,140	M74LS38P
C120	M51954BL	IC141	TC74HCU04P
C121	M74LS373P	IC142,143	M5218P
C122,123	M74LS156P	IC144	M74LS08P
C124	V9338C	IC145	M74LS30P
C129	PD5044	IC146	M74LS32P
C130	M5L8253P-5		
C131	M5L8251AP-5		
C132	M75188P	Q102	2SA933S
C133	M75189AP	D101~109	1S1555
C134	M5W1793-02P		
C135	SED9421C0B		
C136	M74LS74AP		

IC136(2/2), IC141(1/6, 2/6): RS-232C CLOCK GENERATOR

IC134, IC137~IC140: FLOPPY DISK INTERFACE

X101 : ASS-028
X102 : ASS1006
X103 : ASS1007
R105 : RA8S103J
R106 : RA8S153J
R113,114 : RA8S223J
R128 : RA8S472J
R168,169 : RA6S472J
S102 : ASH1010
F101~103 : ATF1010
F104~117 : ATF1011
X104 : ASS1008
TC101 : ACM-021
C102~119,159~171, : ACG-044
C173,174

IC142 (1/2): SOUND MIXING

IC142 (2/2), IC143: CPE DATA READER

IC122, IC123: KEYBOARD INTERFACE

KEY BOARD

IC135: VFO FLOPPY DISK CLOCK GENERATOR

CONNECTOR ASSEMBLY (1)
CONTROLLER 2
CONTROLLER 1

SW ASSEMBLY
S101 : RESET SULL2N

CONTROL I
CONTROL II
ADDRESS BUS
DATA BUS

4. ELECTRICAL PARTS LIST

NOTES:

- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*
  Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).

560Ω	*56 × 10¹*	*561*	*RD1/4PS 5 6 1 J*
47kΩ	*47 × 10³*	*473*	*RD1/4PS 4 7 3 J*
0.5Ω	*0R5*		*RN2H 0 R 5 K*
1Ω	*010*		*RS1P 0 1 0 K*

  Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ	*562 × 10¹*	*5621*	*RN1/4SR 5 6 2 1 F*

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- *For your parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

Miscellaneous Parts

Mark	Symbol & Description	Part No.
	Regulator assembly	AWZ1177
	Filter assembly	
	LED assembly	
	AV SW assembly	AWZ1172
	CPU assembly	AWZ1186
	RGB assembly	
	SW assembly	
	Connector assembly (1)	
	Connector assembly (2)	
⚠	C1,C2 Capacitor (0.01/AC125V)	ACG1003
⚠ ★	T1 Power transformer	ATT1030
⚠★★	S1 Push switch (POWER)	ASG-546
⚠★★	FU1 Fuse (1.6A)	AEK-121
	Floppy disc drive (FLOPPY A)	AXX1004
★★	Fan motor	AXM1004
⚠	AC power cord	ADG1007
⚠	AC cord stopper	AEC1026

Regulator Assembly (AWZ1177)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC11	STR9005
★★	IC12	μPC7812H
★★	IC13	μPC7912H
★★	Q11,Q13	2SA933S
★★	Q12,Q15	2SC1740S
★★	Q14	2SD438(A)
★	D11	RBV602
★	D12	RB152
★	D15	RD15EB
★	D13,D14	1S1555

CAPACITORS

Mark	Symbol & Description	Part No.
	C11−C13 (6800μF/16V)	ACH-382
	C19	CEAS102M16
	C20	CEAS102M25
	C17	CEAS222M25
	C25−C28	CEAS470M25
	C23	CEAS470M50
	C22	CEAS471M16
	C16	CEAS472M6
	C24	CKCYF223Z50 (CKDYF223Z50)
	C14,C15,C18,C21	CQMA104K50

RESISTORS

NOTE:When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

Mark	Symbol & Description	Part No.
	R17	RS1LMF330J
	R11	RS1PMF102J
	Other resistors	RD1/8PM□□□J

Filter Assembly

COIL

Mark	Symbol & Description	Part No.
⚠	L11 Line filter	ATF-168

CAPACITORS

Mark	Symbol & Description	Part No.
⚠	C30,C31 (0.0047μF)	ACG-505
⚠	C29 (0.1μF)	ACG1002

LED Assembly

SEMICONDUCTOR

Mark	Symbol & Description	Part No.
★	D16 LED (POWER)	AEL-460

AV SW Assembly (AWZ1172)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC304	M5218P
★★	IC306	NJM79L05A
★★	IC301−IC303	TC4052BP
★★	IC305	μPC78M05H
★★	Q303	2SA933S
★★	Q301,Q302,Q304−Q307	2SC1740S
★★	Q308,Q309	2SC2878
★	D301−D325	1S1555

CAPACITORS

Mark	Symbol & Description	Part No.
	C328−C333,C335,C336,C339, C340,C346,C347 (0.1μF) C322−C325	ACG-044 (CKDYX104M25) CCCSL101J50 (CCDSL101J50)
	C309	CCCSL220J50 (CCDSL220J50)
	C310−C317	CEAS010M50
	C305,C318,C319,C326,C327	CEAS100M25
	C320,C321	CEAS101M10
	C337	CEAS221M10
	C301−C304,C307,C334,C338, C341	CEAS470M16
	C308	CKCYB222K50 (CKDYB222K50)
	C345	CKCYF223Z50 (CKDYF223Z50)
	C306	CQMA333J50

RESISTORS

NOTE:When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

Mark	Symbol & Description	Part No.
	All resistors	RD1/8PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	6P Terminal	AKB1017

CPU Assembly (AWZ1186)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC201	BA7230LS
★★	IC101	LH0080A
★★	IC113	M5L27128K-FD
★★	IC114	M5L2764K-RS
★★	IC131	M5L8251AP-5
★★	IC130	M5L8253P-5
★★	IC134	M5W1793-02P
★★	IC120	M51954BL
★★	IC142,IC143	M5218P
★★	IC203	M74LS00P
★★	IC137,IC205	M74LS04P
★★	IC144	M74LS08P
★★	IC204	M74LS123P
★★	IC138	M74LS14P
★★	IC122,IC123	M74LS156P
★★	IC107,IC108	M74LS157P
★★	IC106	M74LS245P
★★	IC145	M74LS30P
★★	IC146	M74LS32P
★★	IC102−IC105	M74LS367AP
★★	IC121	M74LS373P
★★	IC139,IC140	M74LS38P
★★	IC136	M74LS74AP
★★	IC132	M75188P
★★	IC133	M75189AP
★★	IC129	PD5044
★★	IC135	SED9421C0B
★★	IC119	S1985
★★	IC141	TC74HCU04P
★★	IC109,IC110,IC125−IC128	MB81464-12 (TMM41464P-12) (M5M4464P-12)
★★	IC111	M5L27256K-MM
★★	IC112	M5L27128K-ME
★★	IC202	V7010
★★	IC124	V9938C
★★	Q211,Q216	DTC124ES
★★	Q102,Q201,Q205,Q206,Q208, Q213,Q215	2SA933S
★★	Q202−Q204,Q207,Q209,Q210, Q212,Q214	2SC1740S
★	D205	ITT310
★	D101−D109,D201−D204	1S1555

SWITCH

Mark	Symbol & Description	Part No.
★★	S102 Slide switch (TEST ROM)	ASH1010

COILS AND FILTERS

Mark	Symbol & Description	Part No.
	L202 Tuning coil	ATG1005
	L201 Axial inductor(4.7μH)	LAU4R7K
	F101−F103 EMI filter	ATF1010
	F104−F117 EMI filter	ATF1011
	F201,F202 Low-pass filter	ATF1012

CAPACITORS

Mark	Symbol & Description	Part No.
	TC101 Ceramic trimmer (10p)	ACM-021
	C102−C119,C159−C171,C173, C174,C213,C223,C225,C229, C232,C241 (0.1μF)	ACG-044 (CKDYX104M25)
	C138,C139	CCCCH100D50 (CCDCH100D50)
	C175	CCCCH120J50 (CCDCH120J50)
	C218	CCCCH150J50 (CCDCH150J50)
	C140,C142	CCCCH220J50 (CCDCH220J50)
	C141,C143,C121	CCCCH270J50 (CCDCH270J50)
	C227	CCCCH680J50 (CCDCH680J50)
	C217,C219	CCCCH820J50 (CCDCH820J50)
	C146−C149	CCCSL101J50 (CCDSL101J50)
	C202	CCCSL220J50 (CCDSL220J50)
	C201	CCCSL221J50 (CCDSL221J50)
	C120	CCCSL390J50 (CCDSL390J50)
	C135	CCCSL470J50 (CCDSL470J50)
	C206−C208	CEANP010M50
	C122,C209−C211,C215,C224, C242	CEAS010M50
	C129,C130,C212,C235	CEAS100M25
	C155−C158	CEAS101M10
	C153,C154,C243	CEAS102M6
	C240	CEAS221M10
	C125−C128,C133	CEAS4R7M50
	C101,C150,C214,C221,C231, C244	CEAS470M10
	C151,C152	CEAS470M16
	C203−C205,C233,C234	CEAS471M6
	C124,C136	CKCYB103K50 (CKDYB103K50)
	C220,C228,C230	CKCYF103Z50 (CKDYF103Z50)

Mark	Symbol & Description	Part No.
	C172	CKCYF472Z50
	C137,C145,C226	CQMA104J50
	C134	CQMA222K50
	C238	CQMA223J50
	C222	CQMA223K50
	C123	CQMA224K50
	C237	CQMA471J50
	C236	CQMA472J50
	C132,C144,C216	CQMA473K50
	C131	CQMA682K50
	C239	CQMA821J50

RESISTORS

NOTE:When ordering resistors,convert the resistance value into code form,and then rewrite the part no.as before.

Mark	Symbol & Description	Part No.
★	VR201 Semi-fixed (4.7k)	VRTB6VS472
	R168,R169	RA6S472J
	R105,R106,R113,R114,R128	RA8S□□□J
	R244	RN1/4PQ2702F
	Other resistors	RD1/8PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
⚠	Lithium battery (3V)	AEX1001
★	X104 Crystal resonator (32.768kHz)	ASS1008
★	X101,X201 Crystal resonator (3.579545MHz)	ASS-028
★	X102 Crystal resonator (3.6864MHz)	ASS1006
★	X103 Crystal resonator (16.000MHz)	ASS1007
	DL201 Delay line	ATL1001
	DL202 Delay line	ATN1006

RGB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	Q310,Q311	2SC1740S
★	D326,D327	1S1555

SWITCH

Mark	Symbol & Description	Part No.
★★	S301 Slide switch (STEREO/MONO)	ASH-031

CAPACITORS

Mark	Symbol & Description	Part No.
	C342,C343	CEAS010M50
	C344	CEAS470M16

RESISTORS

NOTE:When ordering resistors,convert the resistance value into code form,and then rewrite the part no.as before.

Mark	Symbol & Description	Part No.
	All resistors	RD1/8PM□□□J

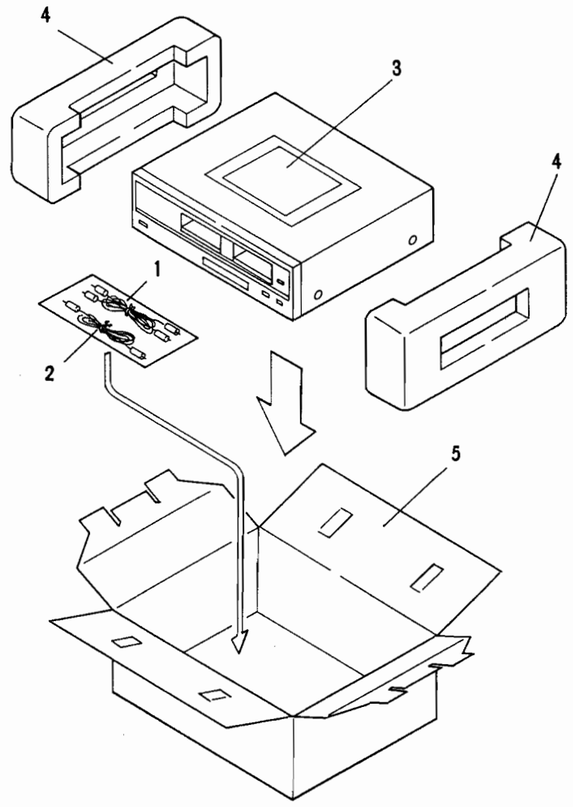
OTHERS

Mark	Symbol & Description	Part No.
	21P Socket (RGB)	AKP1003

5. PACKING

Parts List

Mark	No.	Part No.	Description
	1	ADE-089	Connection cord
	2	ADE-110	Connection cord
	3	ARB1044	Operating instructions (English)
	4	AHA1036	Side pad
	5	AHD1143	Packing case



SW Assembly

SWITCH

Mark	Symbol & Description	Part No.
★★	S101 Push switch (RESET)	SULL2N

Connector Assembly (1)

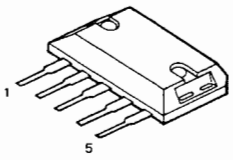
The electrical parts of this assembly are not supplied.

Connector Assembly (2)

The electrical parts of this assembly are not supplied.

External Appearance of Transistors and ICs

STR9005



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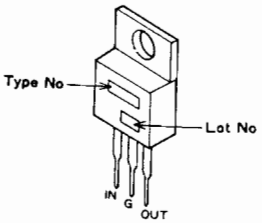
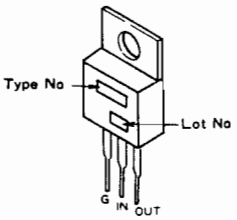
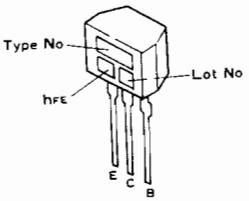
μPC78M05H



μPC7912H



2SA933S
2SC1740S



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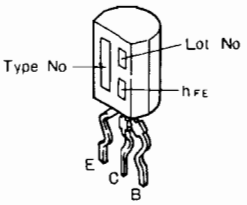
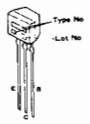
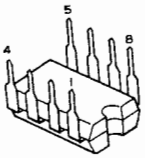


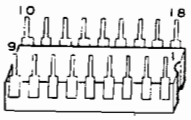
DTC124ES



M5218P



MB81464P-12
TMM41464P-12
M5M44464P-12



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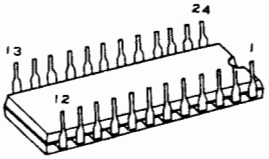

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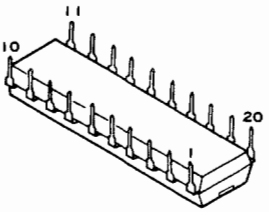

M74LS00P
M74LS04P
M74LS08P
M74LS14P
M74LS30P
M74LS32P
M74LS38P
M74LS74AP
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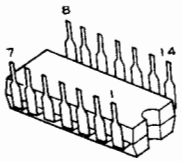
M75189AP
TC74HCU04P



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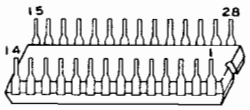
M5L27128K
M5L2718K-FD
M5L2764K-RS
M5L8251AP-5



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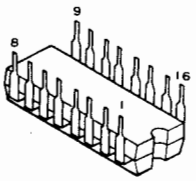
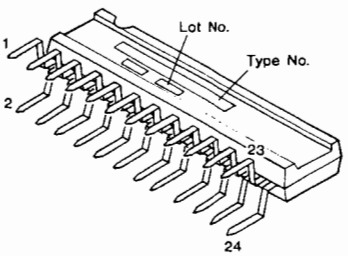
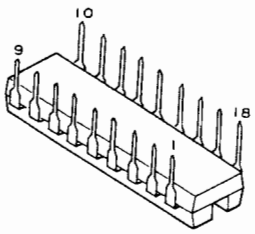
M74LS156P
M74LS157P
M74LS174P
M74LS367AP
TC4052BP



BA7230LS



SED9421COB



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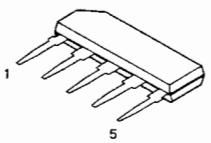
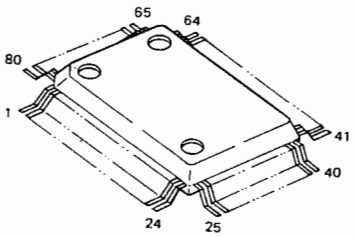
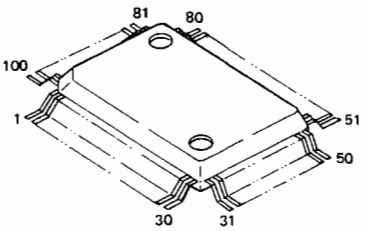


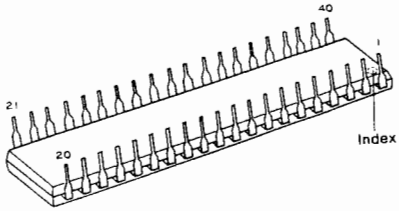
PD5044



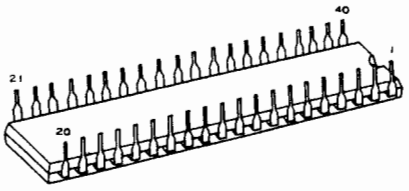
S1985



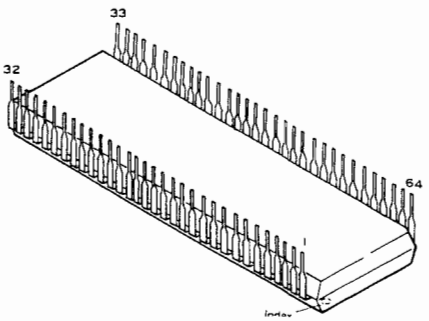
LH0080A



M5W1793-02P



V9938C



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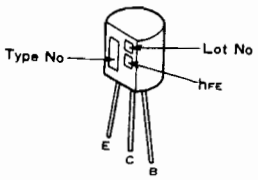

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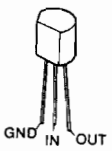


6. ADJUSTMENT PROCEDURES

6.1 Using Test ROM Cartriges

1. Test ROM Selection

The ROM employed depends on whether BASIC is to be run when the power is switched on.

If run : Use BASIC test ROM.
If not run : Use Run test ROM.

2. Using the BASIC Test ROM

○Connect the keyboard, joystick, printer, external video (to VIDEO terminals 1 thru 3 and RGB), and the RS-232C check terminals before switching the power on.

○Get a formatted 3.5-inch 2DD diskette ready.

○Insert the ROM cartridge into the front panel slot and switch the UC-V102 power on (with the diskette not yet inserted).

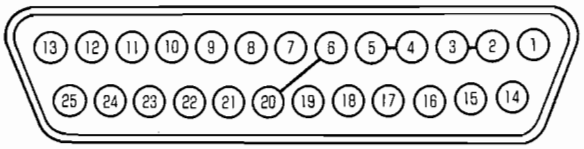
○Insert the diskette into the drive when the test menu appears on the screen.

Test Menu

1 RAM, ROM
2 KEYBOARD
3 SCREEN
4 SOUND
5 CONTROLLER
6 PRINTER
7 FLOPPY
8 RS-232C
9 VIDEO OUTPUT
0 AGING

○The tests selected by pressing the corresponding numbers 1 thru 0 are executed.
After tests 1,2,4,6,7, and 8 are completed, the first menu reappears. (But note that keyboard inputs are required during tests 2 and 4.) During the other tests, the first menu reappears when the specified key is pressed.

RS-232C check terminal pin (male) layout



D SUB 25-PIN (MALE) LAYOUT

Pin numbers and signals
2 ⟶ 3 Data to be transferred
4 ⟶ 5 Data transfer ready
6 ⟶ 20 Data and control signal transfer ready

3. Using the Run Test ROM

○Before switching the power on, open the bonnet and switch the NOR ←→ TEST selector (S102) to the TEST position. Then connect the Centronics check board with the printer cable, and connect the video and audio outputs to the display and amplifier.

○Switch the Centronics check board CONT←→SINGLE selector to the CONT position if running the system continuously, but to the SINGLE position if running one step at a time.

○Insert the ROM into the front panel slot and switch the UC-V102 power on.

Test details

1	STARTING
2	SLOT
3	RAM
4	VRAM
5	CLOCK RAM
6	MSX MAIN ROM
7	MSX EXT ROM
8	RS-232C ROM
9	FDC ROM
10	MAPPER

○ If the result of the starting check is OK, the remaining checks are executed. The results of each check (OK/NG) are displayed after each check is completed. After completing the mapper check, the checks are repeated again started from the slot check.

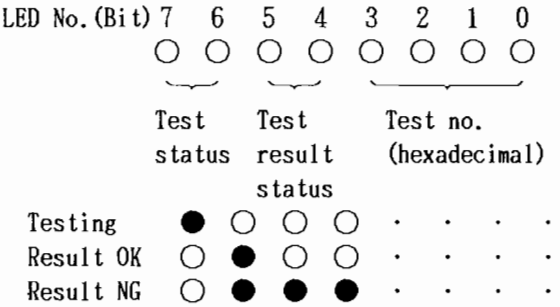
○If the result of the starting check is not OK, a buzzer is activated, the LED on the check board indicate NG status and the check operation is halted.

○The check results are indicated by display, sound, and the Centronics check board.

When OK :
- The screen color is changed to green and "OK" is displayed.
- A high pitched sound is generated by the PSG.
- Only bit 6 out of the upper 4 bit LEDs on the check board comes on.

When NG :
- The screen color is changed to red and"NG"is displayed.
- A low pitched sound is generated by the PSG.
- Bits 6,5, and 4 of the upper 4 bit LEDs on the check board come on.

Centronics check board LEDs



Test numbers and test type

0	STARTING	6	MSX EXT ROM
1	SLOT	7	RS-232C ROM
2	RAM	8	FDC ROM
3	VRAM	B	MAPPER
4	CLOCK RAM	(9,A are not used)	
5	MSX MAIN ROM		

6.2 Adjustments Using Test ROM

(1) Run test ROM

Test item	Test description	Possible cause
Starting	Work RAM 1. Test addresses 8000 to $80FF_H$ and C000 to $C0FF_H$ by galloping method. 2. If a defect is detected, a buzzer is activated, the check board LEDs indicate NG, and the test is stopped. Clock 1. Data is written to and read from registers 0 thru 15. 2. If the read data differs from the written data, a buzzer is activated, the check board LEDs indicate NG, and the test is stopped. PSG 1. Data is written to and read from registers 0 thru 15. 2. If the read data differs from the written data, a buzzer is activated, the check board LEDs indicate NG, and the test is stopped. Slot 1. The primary slot register (port $A8_H$) and secondary slot register ($FFFF_H$) contents are read. 2. Slot numbers are written to and read from the primary and secondary slots register. If the same data as that written to the primary slot register, and data which has been inverted from that written to the secondary slot register cannot be read, a buzzer is activated, the check board LEDs indicate NG, and the test is stopped. 3. Only if the result is OK, $0CC_H$ is written to the primary slot register and 0_H is written to the secondary slot register. The contents are then read with 4000_H and 4001_H, but if the data differs, a buzzer is activated, the check board LEDs indicate NG, and the test is stopped. 4. If the result of step 3 is also OK, the initially read primary and secondary slot register values are written.	Defective RAM Defective S1985 Defective gate array Defective S1985 Defective S1985 Defective S1985
Slot switching	1. The primary slot register (port $A8_H$) and secondary slot register ($FFFF_H$) contents are read. 2, The primary and secondary slots register are switched to various positions. Then 8 bytes are verified from address 0_H or 4000_H and compared with reference data. 3. OK is displayed if the results are OK, but NG is displayed if not OK. 4. The initially read primary and secondary slot register values are written.	Defective S1985

Test item	Test description	Possible cause
RAM	Main RAM 1. Test addresses 0 thru $FFFF_H$ by marching method, and addresses 4000 thru $43FF_H$ by galloping method. 2. If result is OK, OK is displayed and the next test is executed. NG is displayed if not OK, and the test is stopped. VRAM 1. Test addresses 0 thru $1FFFF_H$ by marching method, and addresses 0 thru $51E_H$ by galloping method. 2. OK is displayed if the result is OK, but NG is displayed if not. Clock RAM 1. Test addresses 0 thru $0C_H$ by galloping method. 2. OK is displayed if the result is OK, but NG is displayed if not OK.	Defective RAM Defective S1985 Defective gate array
ROM	MSX EXT MSX FDC RS-232C 1. Divide all ROMs from beginning to end into 256-byte units and determine the check sum. 2. Determine the check sum at each 256 bytes from beginning to end of all ROMs. 3. Compare the respective results with reference data. OK is displayed if OK, and NG if not OK.	Defective RAM Defective gate array
Mapper	1. Read the contents of mapper registers (ports FC thru FF_H). 2. Write 0 thru 15 from mapper registers, and then read. 3. If no defects are detected, append the same mapper register pages to addresses 4000 thru $7FFF_H$ and 8000 thru $BFFF_H$, write data to 4000_H and read data from 8000_H. And also append the same mapper register pages to addresses 0 thru $3FFF_H$ and $C000_H$ thru $FFFF_H$, write data to 0_H, and read data from at $C000_H$. 4. The circuits are normal if the read data is the same as the written data. 5. OK is display if results are OK, but NG is displayed if not OK. 6. Restore the original mapper register values.	Defective S1985

(2) BASIC Test ROM

Test item	Test description	Possible cause
RAM and ROM	RAM 1. Divide the test area into sections 0 thru $3FFF_H$, 4000 thru $7FFF_H$, 8000 thru $BFFF_H$, and C000 thru $FFFE_H$. 2. Read and write data sequentially from the lead address. Then read the written data and check that it matches the originally read data. 3. OK or ERROR is displayed, and the next test is then executed. ROM 1. The ROMs tested are the BASIC and EXT-BASIC ROMs. 2. Determine the check sum of each 256 bytes of data in the respective ROMs and compare the results with reference data. 3. OK or ERROR is displayed, and the next test is then executed.	Defective RAM Defective S1985 Defective gate array Defective ROM Defective gate array
Keyboard	1. Enter the specified keys from the keyboard. 2. OK is displayed if the keys read by the computer are the same as the specified keys. ERROR is displayed if not.	Defective keyboard circuit Defective S1985 Defective I/F IC Defective cable
Screen	WIDTH: Change the number of characters displayed along the X axis in text mode at every 10 characters from character 10 to 80 on SCREEN 0, and from character 12 to 32 on SCREEN 1, and display the character at each change. COLOR BAR: Display the 16-color color bar on SCREEN 2. MULTI-COLOR: Display points(blocks)on SCREEN 3. 512 LINE: Display 512 lines on SCREEN 7. COLOR SPRITE: Display color sprite on SCREEN 7. PAGE SWITCH: Display pages 0 and 1 alternately on SCREEN 7. 256 COLOR LINE: Display 256-color line on SCREEN 8. COLOR SPRITE: Display color sprite on SCREEN 8. Specified color codes are same as on SCREEN 7.	Defective S1985 Defective V9938 Defective VRAM

Test item	Test description	Possible cause
SOUND	1. Generate audio and "audio plus" noise signals in Ach, Bch, and Cch in that order. 2. Generate sound effects each time the space bar is pressed.	Defective S1985 Defective gate array Defective analog circuit
CONTROLLER	1. Select the port number of the port to be tested. 2. Display numbers 1 thru 8 on the screen in the joystick direction. 3. Change character color each time the trigger button is pressed.	Defective S1985
PRINTER	Print out characters to printer.	Defective S1985
FLOPPY	1. Save data in sequential file, and then load that data. (Repeat three times.) 2. Save data in random access file, and then load that data. (Repeat three times.) 3. OK is displayed if the data saved in steps 1 and 2 is the same as the respective load data. ERROR is displayed if the data is different.	Defective VFO Defective drive Defective gate array Defective FDC ROM Defective I/F IC Defective diskette
RS-232C	1. Connect the RS-232C check terminals. 2. Pass data from the RS-232C output terminal to the input terminal. OK is displayed if the data is the same, but ERROR is displayed if the data is not the same.	Defective gate array Defective RS-232C RS-232C ROM Defective I/F IC
VIDEO OUTPUT	1. Apply external video signals to VIDEO 1 thru 3 and RGB. 2. Display an 8-color color bar and make the top half transparent. Then using function keys, switch to the computer, superimpose, video, external video, full tone, and half tone positions.	Defective gate array Defective analog circuit
AGING	Test ROMs and RAMs. Execute the screen test (but without displaying the selection screen). Execute the floppy test. Execute the RS-232C test. Execute the video test (but without displaying the selection screen). Repeat the above tests.	

6.3 Floppy Test ROM

1. Usage

○Inserted into the front panel slot of the UC-V102, the floppy test ROM is used to test the floppy disk drive and floppy disk controller.

○Before commencing these tests, a 3.5-inch 2DD diskette must first be formatted.

Formatting procedure

Using a UC-V102 unit which is functioning properly, switch the power on, insert a diskette into drive A, and key in "CALL FORMAT" from the keyboard.
Key in A in response to the drive no. enquiry, and 2 (double-sided 9-sector) as the diskette type.
Then wait until OK appears on the screen to indicate end of formatting.

(1) Set the ROM cartridge in the front panel slot and switch the UC-V102 power on. (Do not insert the diskette at this stage.)

(2) When the following message appears on the screen after a little while, insert the formatted diskette into drive A, and press the RESET switch.

The following message appears if the test is started without first inserting a diskette.

```
FDD NOT READY
INSERT FLOPPY DISK TO FDD
THEN PUSH RESET SWITCH !!
```

(3) When the RESET switch is pressed, the following test menu is displayed. And soon as a number from 1 to 5 is keyed in, the selected test is executed.

If steps (1) and (2) are executed in the following manner, the test menu appears without being preceded by the NOT READY message.

(i) Set the ROM cartridge → (ii) switch power on → (iii) insert diskette soon after switching the power on.

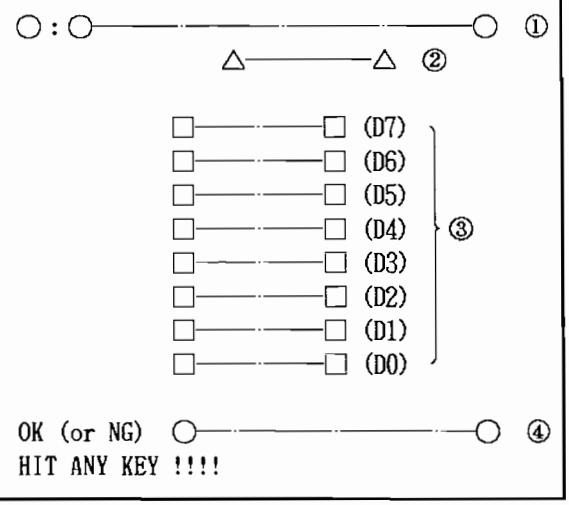
Test menu

```
FLOPPY TEST PROGRAM
1 : FDC REGISTER READ / WRITE
2 : DRIVE MOTOR ON AND READY
3 : SEEK AND BUSY ON / OFF
4 : READ / WRITE / VERIFY
5 : LIFE TEST

KEY IN 1-5
```

(4) When the above test menu appears, key in a number from 1 to 5 to execute the corresponding test. The test menu is replaced immediately by the following type of display. And when the test is completed, FDC (floppy disk controller) status is displayed with OK or NG.
Press any key to return to the test menu and proceed to the next test.

Screen display at end of one test (excluding test 5)

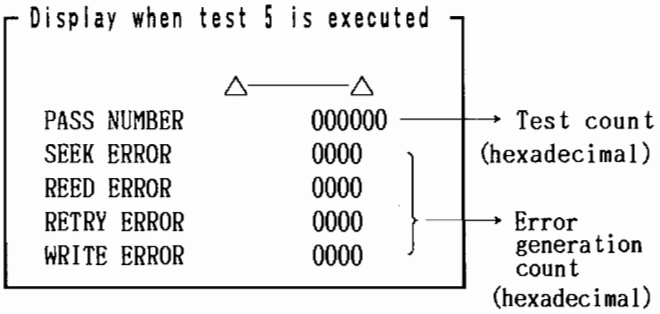


① Test name displayed when test is started.

② READ, WRITE, SEEK displayed when executing test 4.

③ The meaning of the FDC status bit is displayed when the bit is 1, and − is displayed when 0. The cause of the problem is indicated if a * is displayed.

④ OK or NG is displayed with related messages.



Display when test 5 LIFE TEST is executed

The life test consists of continuous execution of READ / WRITE / VERIFY operations. The RESET switch must be pressed to stop this life test. The count display is expressed in hexadecimal notation with numerals from 0 to 9 and alphabetical characters A thru F.

2. Test Details

(1) FDC REGISTER READ/WRITE

○Write data 00H thru FFH to the FDC data, sector, and track registers, and then read to check that data contents have been correctly written, and also to check that the interface between FDC and CPU is functioning properly.
○Although * NOT READY is displayed after the test has been completed, this message has no meaning.

(2) DRIVE MOTOR ON AND READY

○Check the time taken for the drive motor to reach READY status after the motor is switched on. The result is NG if the specifications rating of 700 msec is exceeded.
○READY status is not achieved (NG) if a diskette is not inserted.
○If the diskette write protect notch is open, a status message is displayed. The drive write protect sensor circuit can also be tested in this way.

(3) SEEK AND BUSY ON/OFF

○Check that SEEK operations are executed correctly in both directions between tracks 0 and 79, and that BUSY status is indicated the drive is operating.
○The unit waits is standby mode if a diskette has not been inserted. Operation is commenced as soon as a diskette is inserted.
○NG is displayed if an unformatted diskette is inserted.

(4) READ/WRITE/VERIFY

○Random data is written and read to and from tracks 0 thru 79 in sector 1 on sides 0 and 1. The written and read data is then compared.
○This also serves as a general test of the folppy disk drive and diskette.
○The unit waits is standby mode if a diskette has not been inserted. Operation is commenced as soon as a diskette is inserted.

(5) LIFE TEST

○Random data is written sequentially to all tracks 0 thru 79 in all sectors 1 thru 9 and on both sides 0 and 1. (Read/verify is also executed at this stage.) After, track, sector, and side are specified at random, data is read and compared, and then re-write, re-read, and re-compared again to check for the existence of errors. This operation is repeated endlessly.
○The unit waits is standby mode if a diskette has not been inserted. Operation is commenced as soon as a diskette is inserted.
○The test cannot be executed if a write-protected diskette is inserted.

CAUTION!!

The diskette used with this test ROM should be reserved for test purposes only. If a diskette containing BASIC and other programs is used, those programs will be permanently erased.

3. Status Message Meanings and Likely Cause of Trouble

(Messages marked by an asterisk indicate trouble)

Status message	Meaning	Likely cause
* NOT READY	Drive is not ready to operate.	READY status not achieved if motor fails to start when diskette is inserted. +12V line, motor, or motor driver.
WRITE PROTECT	Diskette is write-protected.	Write protect status is cancelled by sliding the write protect notch to cover the hole.
* SEEK ERROR	Diskette ID field cannot be found, or ID field track and sector numbers do not correspond with head position.	Defective diskette (scratched surface, or unformatted), or drive head or step motor drive stage or drive circuit.
* CRC ERROR	ID field read error generated.	Defective diskette (scratched surface, or unformatted), or drive head.
ON TRACK 0	Head is at track 0.	———
FOUND INDEX	Index hole detected.	———
BUSY/COMMAND EXCUTE	FDC is executing a command.	———
* WRITE FAULT	Write operation aborted.	Software problem, or defective FDC.
* RECORD ID NOT FOUND	ID field contain specified track, side, and sector numbers does not exist.	Defective diskette (scratched surface, or unformatted), or drive head.
* LOST DATA ERROR	The prescribed quantity of data was not read or written in the prescribed time.	Software problem, or defective FDC or VFO.
———	No status established.	———

7. IC DATA

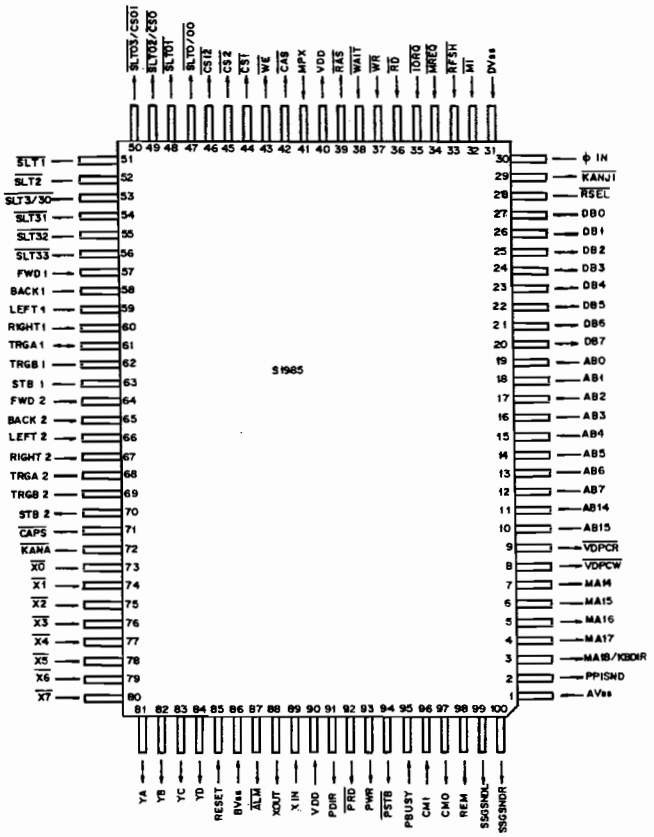
■S1985 (IC119)

MSX$_2$ system LSI

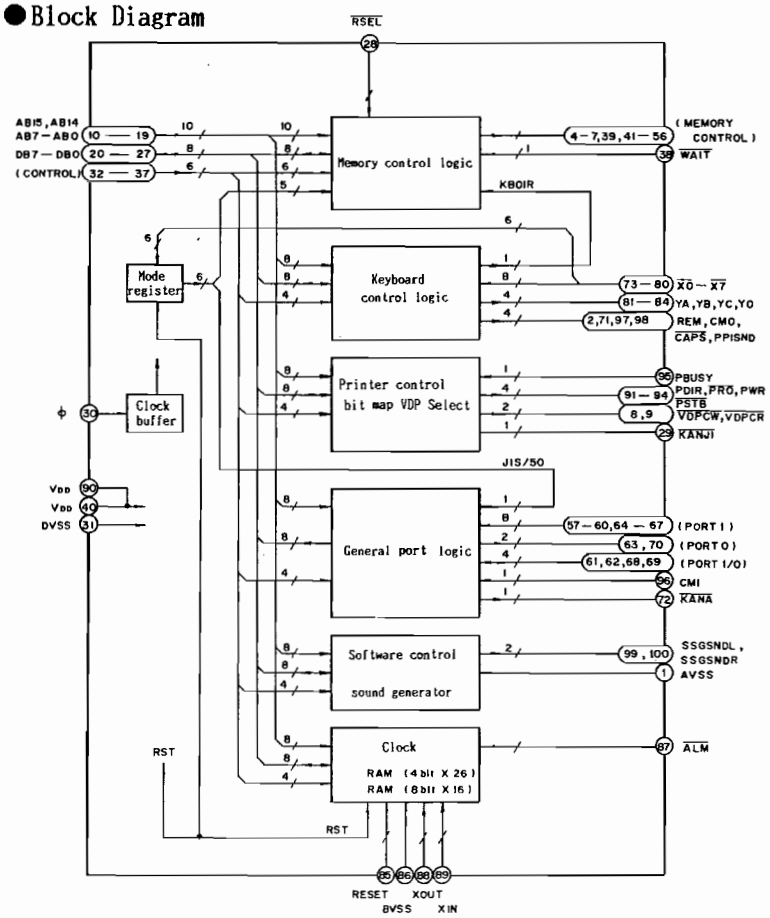
The S1985 LSI developed for the MSX$_2$ is used in memory control, and in control of the VDP, keyboard, printer, and other peripherals. And with an extension capacity based on MSX$_2$ specifications, this LSI also includes a built-in clock and SSG(PSG) stage capable of generating musical signals. The main features are listed below.

1. Simultaneous extension and control of slots 0 and 3
2. Mapper function (max. 256K bytes)
3. VDP access (1 WAIT request when reading/writing)
4. RAM access (RAS only refresh selection)
5. Keyboard I/F
6. Printer I/F
7. General port (CONTROLLER 1,2) control
8. SSG(PSG) and PPI output
9. MSX$_2$ standard clock functions
10. MSX$_2$ standard back-up RAM (4 bits × 26)

●Pin Connections (Top View)



●Block Diagram



●Pin Functions

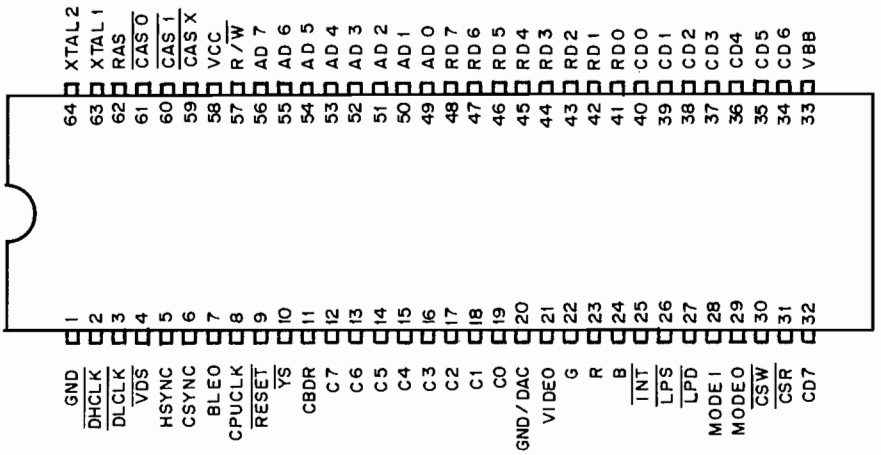
No.	Symbol	Function
1	AVss	GND for sound
2	PPISND	PPI sound signal output
3	MA_{18}/KBDIR	Upper address or keyboard bus direction signal output
4	MA_{17}	Mapper address signal output
5	MA_{16}	
6	MA_{15}	
7	MA_{14}	
8	$\overline{VDPCW}$	VDP write signal output
9	$\overline{VDPCR}$	VDP read signal output
10	AB_{15}	Z80ACPU address input
11	AB_{14}	
12	AB_7	
13	AB_6	
14	AB_5	
15	AB_4	
16	AB_3	
17	AB_2	
18	AB_1	
19	AB_0	
20	DB_7	Z80ACPU data input/output
21	DB_6	
22	DB_5	
23	DB_4	
24	DB_3	
25	DB_2	
26	DB_1	
27	DB_0	
28	$\overline{RESL}$	Extension slot designation register control signal input
29	$\overline{KANJI}$	(Kanji ROM select signal output)
30	ϕ IN	Clock signal input
31	DVss	0V (GND)
32	M_1	Z80ACPU $\overline{M_1}$ input
33	$\overline{RFSH}$	Z80ACPU $\overline{RFSH}$ input
34	$\overline{MREQ}$	Z80ACPU $\overline{MREQ}$ input
35	$\overline{IORQ}$	Z80ACPU $\overline{IORQ}$ input
36	$\overline{RD}$	Z80ACPU $\overline{RD}$ input
37	$\overline{WR}$	Z80ACPU $\overline{WR}$ input
38	$\overline{WAIT}$	$\overline{WAIT}$ signal output to Z80ACPU (wired logic enabled)
39	$\overline{RAS}$	DRAM RAS signal output
40	V_{DD}	+5V
41	MPX	DRAM address multiplex signal output
42	$\overline{CAS}$	DRAM $\overline{CAS}$ signal output
43	$\overline{WE}$	DRAM $\overline{WE}$ signal output
44	$\overline{CS_1}$	ROM select 4000H thru 7FFFH signal output
45	$\overline{CS_2}$	ROM select 8000H thru BFFFH signal output
46	$\overline{CS_{12}}$	ROM select 4000H thru BFFFH signal output
47	$\overline{SLT_{00}}$/$_{00}$	SLOT#0 or SLOT#00 select signal output
48	$\overline{SLT_{01}}$	SLOT#01 select signal output
49	$\overline{SLT_{02}}$/$\overline{CS_0}$	SLOT#02 select or ROM select 0000H thru 3FFFH signal output
50	$\overline{SLT_{03}}$/$\overline{CS_{01}}$	SLOT#03 select or ROM select 0000H thru 7FFFH signal output

No.	Symbol	Function
51	$\overline{SLT_1}$	SLOT#1 select signal output
52	$\overline{SLT_2}$	SLOT#2 select signal output
53	$\overline{SLT_3}$/$_{30}$	SLOT#3 or SLOT#30 select signal output
54	$\overline{SLT_{31}}$	SLOT#31 select signal output
55	$\overline{SLT_{32}}$	SLOT#32 select signal output
56	$\overline{SLT_{33}}$	SLOT#33 select signal output
57	FWD_1	Joystick FWD signal input (general port input)
58	$BACK_1$	Joystick BACK signal input (general port input)
59	$LEFT_1$	Joystick LEFT signal input (general port input)
60	$RIGHT_1$	Joystick RIGHT signal input (general port input)
61	$TRGA_1$	Joystick TRGA signal input (general port input)
62	$TRGB_1$	Joystick TRGB signal input (general port input)
63	STB_1	General port output
64	FWD_2	Joystick FWD signal input (general port input)
65	$BACK_2$	Joystick BACK signal input (general port input)
66	$LEFT_2$	Joystick LEFT signal input (general port input)
67	$RIGHT_2$	Joystick RIGHT signal input (general port input)
68	$TRGA_2$	Joystick TRGA signal input (general port input)
69	$TRGB_2$	Joystick TRGB signal input (general port input)
70	STB_2	General port output
71	$\overline{CAPS}$	CAPS LED signal output
72	$\overline{KANA}$	KANA LED signal output
73	$\overline{X_0}$	Keyboard return signal input
74	$\overline{X_1}$	
75	$\overline{X_2}$	
76	$\overline{X_3}$	
77	$\overline{X_4}$	
78	$\overline{X_5}$	
79	$\overline{X_6}$	
80	$\overline{X_7}$	
81	Y_A	Keyboard drive signal output
82	Y_B	
83	Y_C	
84	Y_D	
85	RESET	Reset signal input
86	BV_{SS}	Clock back-up power supply
87	$\overline{ALM}$	Alarm signal output
88	XOUT	Output to clock oscillator
89	XIN	Input from clock oscillator
90	V_{DD}	+5V
91	PDIR	Printer direction signal output
92	$\overline{PRD}$	Printer read signal output
93	$\overline{PWR}$	Printer write signal output
94	$\overline{PSTB}$	Printer strobe signal output
95	PBUSY	Printer busy signal input
96	CMI	Cassette read signal input
97	CMO	Cassette write signal output
98	REM	Cassette control signal output
99	SSGSNDL	SSG sound LEFT signal output
100	SSGSNDR	SSG sound RIGHT signal output

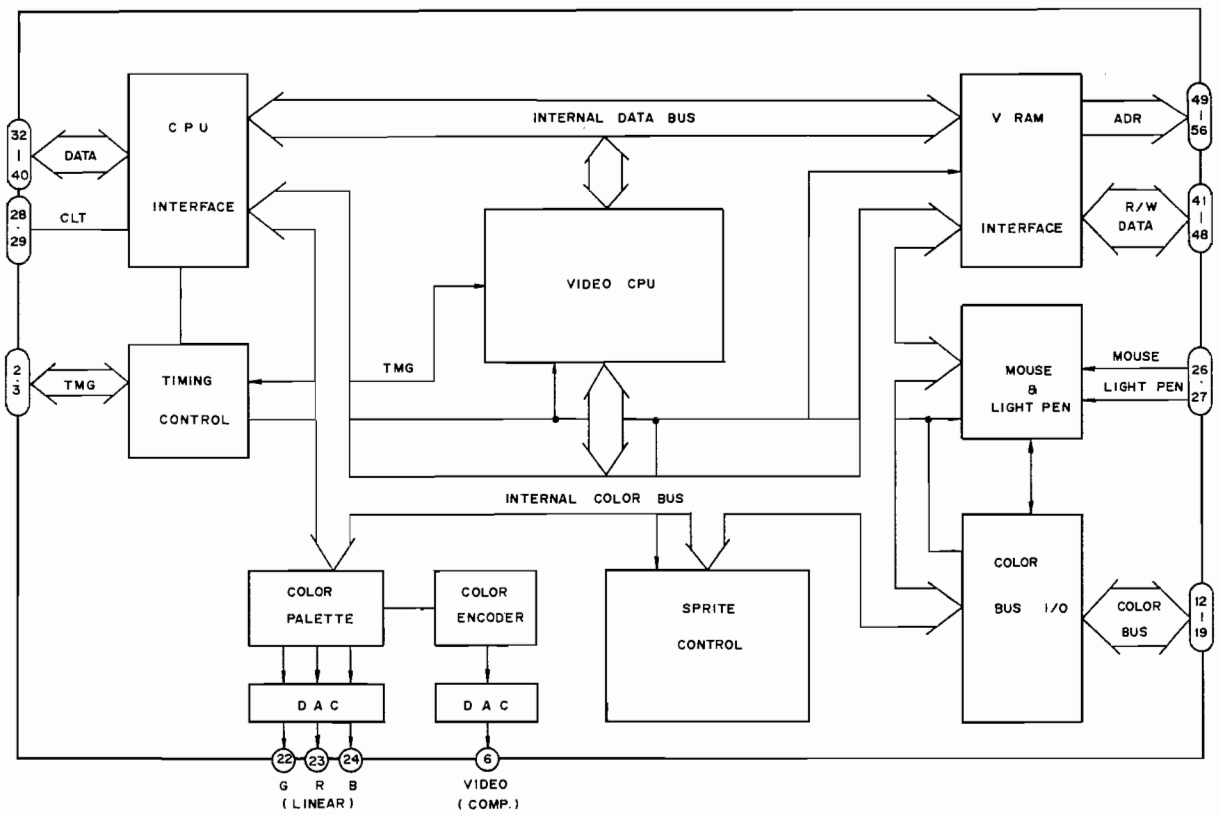
■V9938C (IC124)

MSX$_2$ VDP LSI

● Pin Connections (Top View)



● Block Diagram



● Pin Functions

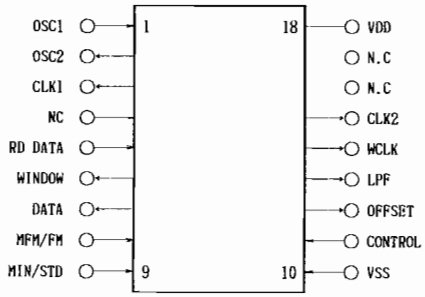
No.	Symbol	Function
1	GND	Ground 0V
2	$\overline{\text{DHCLK}}$	Dot clock output at high resolution Approx. 10.74MHz open drain output
3	$\overline{\text{DLCLK}}$	Dot clock output at low resolution Approx. 5.37MHz open drain output
4	$\overline{\text{VDS}}$	VRAM data select $\overline{\text{VDS}}$ = Low ; VRAM access for display data purposes $\overline{\text{VDS}}$ = High ; VRAM access for other purposes
5	HSYNC	3-value logic with output of upper levels (high to middle) and input of lower levels (middle to low). High ; Timing apart from HSYNC, or color burst timing Middle ; Timing apart from HSYNC, or color burst Low ; HSYNC timing
6	CSYNC	3-value logic with composite upper level SYNC output, and VSYNC input lower level
7	BLEO	3-value output indicating 1st field / 2nd field blanking Open drain output High ; 2nd Field active Middle ; 1st Field active Low ; Return line blanking interval
8	CPUCLK	Output of frequency 1/6 of XTAL
9	$\overline{\text{RESET}}$	Resetting of all circuits in VDP to initial status
10	$\overline{\text{YS}}$	Signal used to switch VDP RGB output and external video signal (during superimposing operations) YS = High ; VDP output transparent YS = Low ; VDP output not transparent
11	CBDR	Pin indicating color bus direction High ; Color bus input Low ; Color bus output
12	C7 MSB	Color bus Normally used as input ports when color code output is digitized. Four upper bits are also used as mouse inputs. C4 = XA C5 = XB C6 = YA C7 = YB
13	C6	
14	C5	
15	C4	
16	C3	
17	C2	
18	C1	
19	C0 LSB	
20	GND DAC	Ground 0V
21	VIDEO	Composite video signal output
22	G	Linear RGB signal output
23	R	
24	B	
25	$\overline{\text{INT}}$	CPU interrupt output, open drain output Interrupt generated when low
26	$\overline{\text{LPS}}$	Light pen switch input. Mouse switch input when mouse is used. Low ; Switch ON High ; Switch OFF

No.	Symbol	Function
27	$\overline{\text{LPD}}$	Light pen sensor output/input. Mouse switch input when mouse is used. Low ; Light detected, or switch ON High ; Otherwise
28	MODE 1	CPU interface mode select
29	MODE 0	
30	$\overline{\text{CSW}}$	CPU-VDP write strobe
31	$\overline{\text{CSR}}$	CPU-VDP read strobe
32	CD7 MSB	CPU data bus
33	VBB	Circuit board voltage
34	CD6	CPU data bus
35	CD5	
36	CD4	
37	CD3	
38	CD2	
39	CD1	
40	CD0 LSB	
41	RD0 LSB	VRAM data bus
42	RD1	
43	RD2	
44	RD3	
45	RD4	
46	RD5	
47	RD6	
48	RD7 MSB	
49	AD0 LSB	VRAM address bus
50	AD1	
51	AD2	
52	AD3	
53	AD4	
54	AD5	
55	AD6	
56	AD7 MSB	
57	R / $\overline{\text{W}}$	VRAM write strobe
58	VCC	Line 5V
59	$\overline{\text{CAS X}}$	VRAM column address strobe X (for extension VRAM)
60	$\overline{\text{CAS 1}}$	VRAM column address strobe 1 (VRAM front half)
61	$\overline{\text{CAS 0}}$	VRAM column address strobe 0 (VRAM rear half)
62	$\overline{\text{RAS}}$	VRAM row address strobe
63	XTAL 1	This pin is connected to XTAL. Externally generated clocks are also applied to this pin.
64	XTAL 2	

■SED9421COB (IC135)

Data separator VFO IC

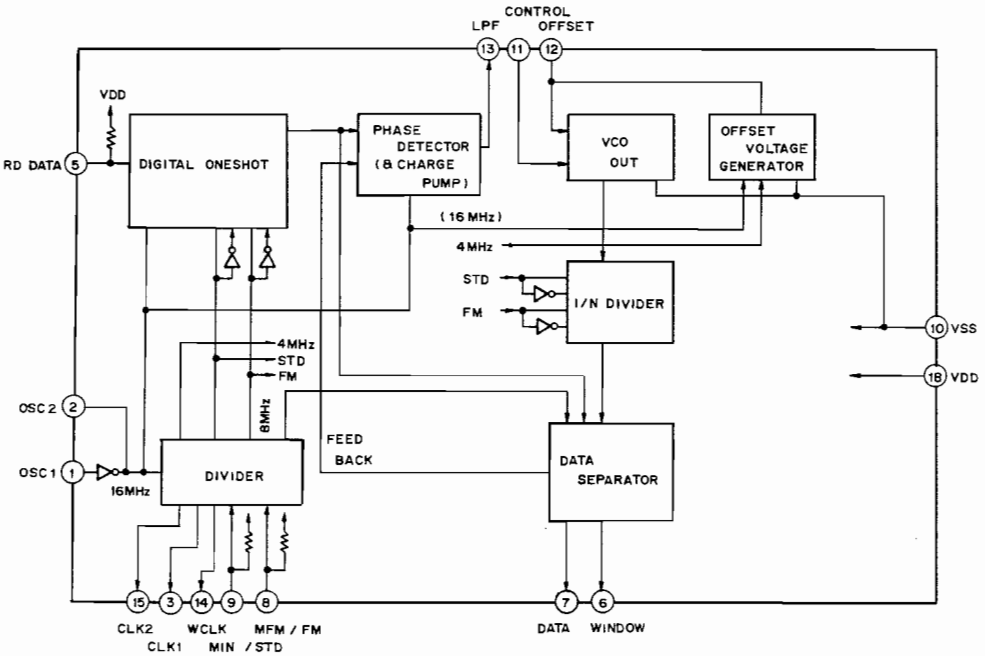
●Pin Connections (Top View)



●Pin Functions

No.	Symbol	Function
1	OSC1	(1) Inverter amplifier gate input in crystal osccilator circuit (2) Input pin used for 16MHz external clock input
2	OSC2	(1) Inverter amplifier drain output in crystal osccilator circuit
3	CLK1	FDC clock ・Standard floppy (8-inch) ; 8MHz ・Mini floppy (5-inch) ; 4MHz
4	NC	Not connected
5	RD DATA	Input pin for read data signal from floppy disk drive (FDD) (with pull-up resistor)
6	WINDOW	Output pin for data window signal used to separate DATA signal into clock and data pulse signals.
7	DATA	Output pin for data signal obtained from the RD DATA signal. This output is read to FDC and separated into data and clock pulse signals by the WINDOW signal.
8	MFM/$\overline{FM}$	Double/single density recording selector pin (with pull-up resistor) ・Double density (MFM recording) ; High level ・Single density (FM recording) ; Low level
9	MIN/$\overline{STD}$	Mini floppy disk (5-inch) / standard floppy disk (8-inch) selector pin (with pull-up resistor) ・5-inch floppy ; High level ・8-inch floppy ; LOW level
10	Vss	Ground pin
11	CONTROL	Voltage Controlled Oscillator (VCO) control voltage (loop filter output voltage) input pin
12	OFFSET	Offset voltage input pin for compensation of oscillator center frequency in VCO. Automatic generation of offset voltage enabled by external capacitance.
13	LPF	Loop filter connector pin (charge pump output pin)
14	WCLK	FDC (μPD765) write clock ・STD (8-inch)/MFM ; T = 1μsec ・STD/FM ; T = 2μsec ・MIN/MFM ; T = 2μsec ・MIN/FM ; T = 4μsec
15	CLK2	Clock output pin for FD179 FDC ・8-inch floppy ; 2MHz ・5-inch floppy ; 1MHz
16		Not connected
17		
18	V_{DD}	+5V line voltage pin

●Block Diagram



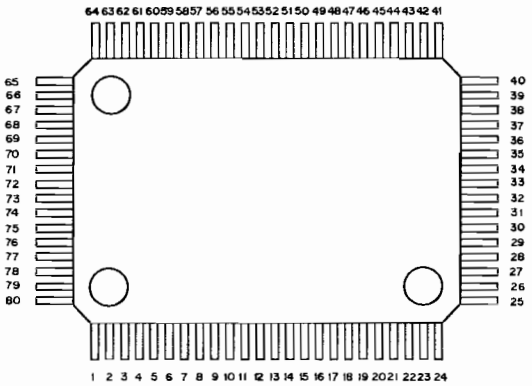
■PD5044 (IC129)

Gate array IC

Functions

1. RAM A7 generator
2. Mapper RAM CAS generator
3. Video muting
4. CPU bus direction circuit
5. Audio/video input selector
6. I/O mask ciruit
7. RMUTE, LMUTE, YM, and AVC circuits
8. (Kanji ROM control circuit)
9. RS-232C control circuit
10. Floppy disk control circuit
11. Superimpose/synchronize mode selector

●Pin Connections (Top View)

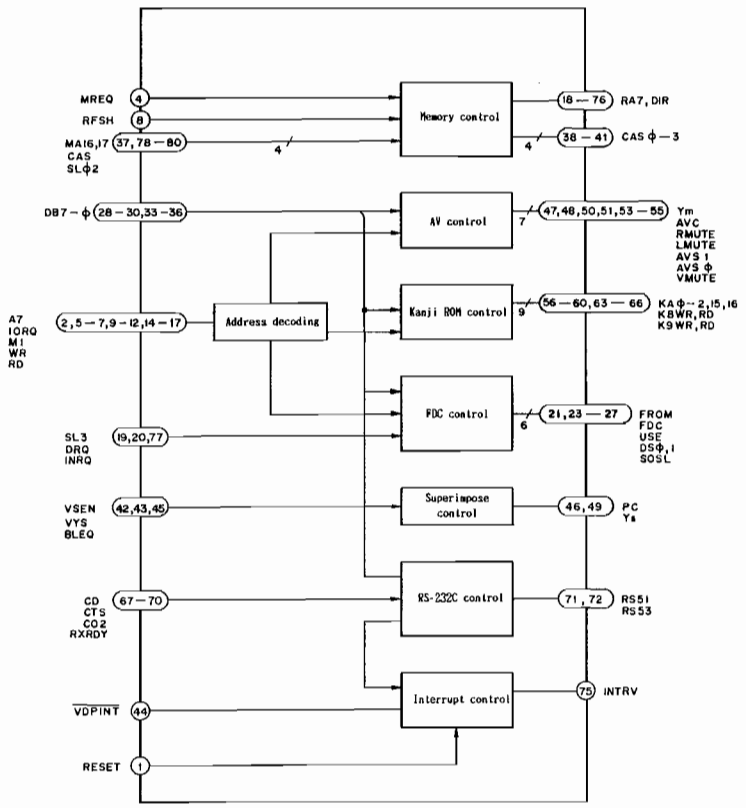


●Pin Functions

No.	Symbol	Function
1	$\overline{RESET}$	SYSTEM RESET
2	$\overline{IORQ}$	Z-80 CPU $\overline{IORQ}$
3	NC	
4	$\overline{MREQ}$	Z-80 CPU $\overline{MREQ}$
5	$\overline{RD}$	Z-80 CPU $\overline{RD}$
6	$\overline{WR}$	Z-80 CPU $\overline{WR}$
7	$\overline{MI}$	Z-80 CPU $\overline{MI}$
8	$\overline{RFSH}$	Z-80 CPU $\overline{RFSH}$
9	AB0	ADDRESS BUS A0
10	AB1	ADDRESS BUS A1
11	AB2	ADDRESS BUS A2
12	AB3	ADDRESS BUS A3
13	NC	
14	AB4	ADDRESS BUS A4
15	AB5	ADDRESS BUS A5
16	AB6	ADDRESS BUS A6
17	AB7	ADDRESS BUS A7
18	RA7	Main RAM A7 signal A6 divided by 2 when refreshed
19	INRQ	FDC INTRQ
20	DRQ	FDC DRQ
21	$\overline{FDC}$	FDC Chip Select Slot30, 7FF8H thru 7FFBH active
22	NC	
23	$\overline{FDROM}$	DISK BASIC ROM chip enable output Slot30, 4000H thru 7FF7H active
24	DS0	FDD Drive Select Slot30 7FFD BIT 1 0 (when bit 7 is H) 0 0 DS0 0 1 DS1
25	DS1	
26	SOSL	FDD Side One Select Slot30 7FFC BIT 0 H:Side One
27	INUSE	FDD Motor ON Controll Slot30 7FFD BIT 7 H:Motor ON
28	DB0	DATA BUS D0
29	DB1	DATA BUS D1
30	DB3	DATA BUS D3
31	TEST	KA0 thru KA16 test pin
32	NC	
33	DB4	DATA BUS D4
34	DB5	DATA BUS D5
35	DB6	DATA BUS D6
36	DB7	DATA BUS D7
37	$\overline{CAS}$	S1985 $\overline{CAS}$
38	$\overline{CAS0}$	Main RAM CAS signal
39	$\overline{CAS1}$	Mapper RAM CAS signal
40	$\overline{CAS2}$	
41	$\overline{CAS3}$	
42	BLEO	VDP BLEO
43	$\overline{VDPYS}$	VDP $\overline{Ys}$
44	$\overline{VDPINT}$	VDP $\overline{INT}$
45	VSENSE	Video Sence In H:External video detected
46	PC/$\overline{EXT}$	INT/EXT Synchronization switching I/O F7H bits 6 & 7 EX-OR VSENSE NAND output

No.	Symbol	Function
47	AVC	AV Controll I/O F7H Bit4 L:TV Interval
48	Ym	Ym Controll I/O F7H Bit5 H:Half tone
49	Ys	Superimpose switching H:Computer EXT・VDPYS・BLEO
50	VMUTE	Video MUTING Reset by $\overline{FDC}$ or $\overline{INTVDP}$×160
51	AVSW1	AV Input Select I/O 50H Bit 1 0 0 0 RGB21pin 0 1 Video 1(Init) 1 0 Video 2 1 1 Video 3
52	NC	
53	AVSW2	AV Input Select I/O 50H Bit 1 0 0 0 RGB21pin 0 1 Video 1(Init) 1 0 Video 2 1 1 Video 3
54	RMUTE	Audio Rch MUTING I/O F7H Bit0 H:MUTE
55	LMUTE	Audio Lch MUTING I/O F7H Bit1 L:Non MUTE
56	$\overline{KR8W}$	(Reserved for kanji ROM)
57	$\overline{KR9W}$	
58	$\overline{KR8R}$	
59	$\overline{KR9R}$	
60	KA16	(Reserved for kanji ROM)
61	NC	
62	NC	
63	KA15	(Reserved for kanji ROM)
64	KA2	
65	KA1	
66	KA0	
67	$\overline{CTS}$	RS-232C CTS
68	CO#2	8253 OUT2
69	CD	RS-232C DCD
70	RxRDY	8251 RDY
71	$\overline{RS8253}$	8253 Chip Select / I/O F5H
72	$\overline{RS8251}$	8251 Chip Select (Mask by bit 5 L:Mask)
73	NC	
74	$\overline{RSEL}$	A8~A13 Decode In
75	INTRV	Interrupt Out $\overline{INTVDP}$ and $\overline{RxRDY}$ OR output RxRDY I/O 82H Mask by bit 0 (H)
76	DIR	Data Bus Controll H by read or interrupt fetch
77	$\overline{SL30}$	S-1985 $\overline{SL30}$
78	$\overline{SL02}$	S-1985 $\overline{SL02}$
79	MA17	S-1985 MA17
80	MA16	S-1985 MA16

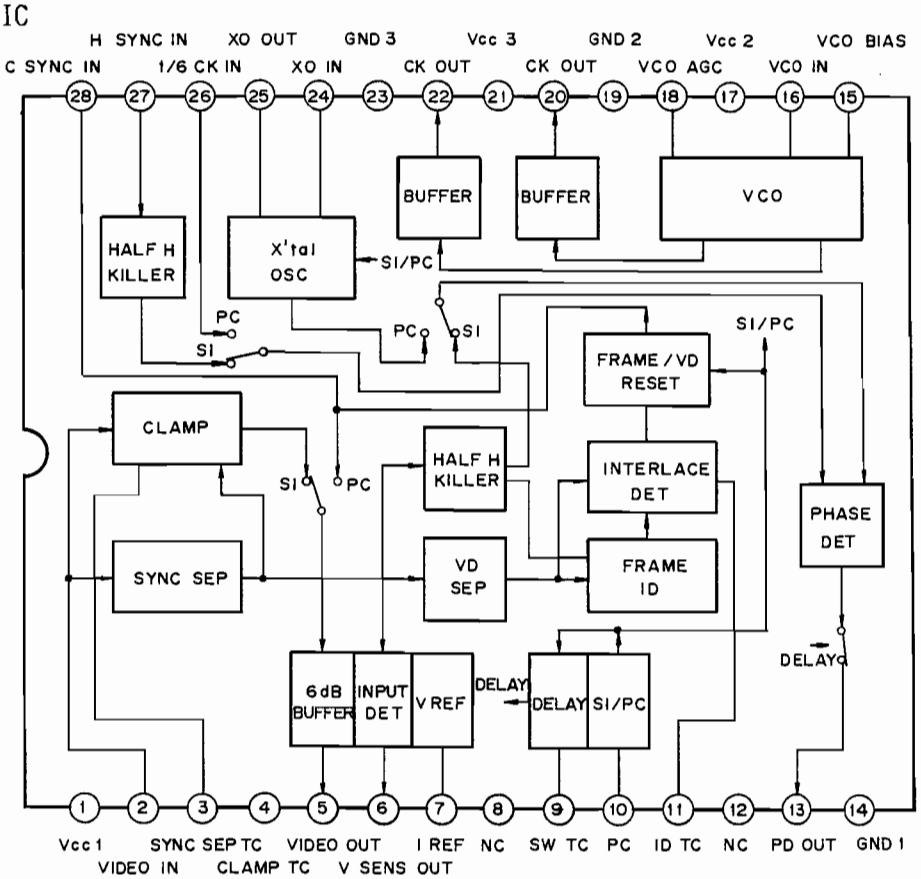
● Block Diagram



■V7010 (IC202)

Bipolar silicon monolithic IC

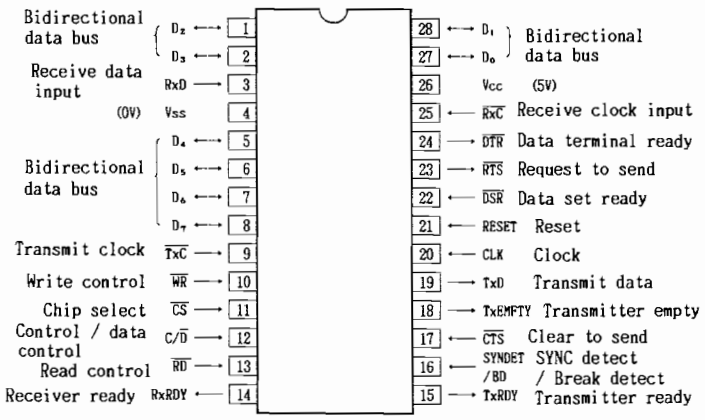
● Block Diagram



■M5L8251AP-5 (IC131)

Programmable communication interface IC

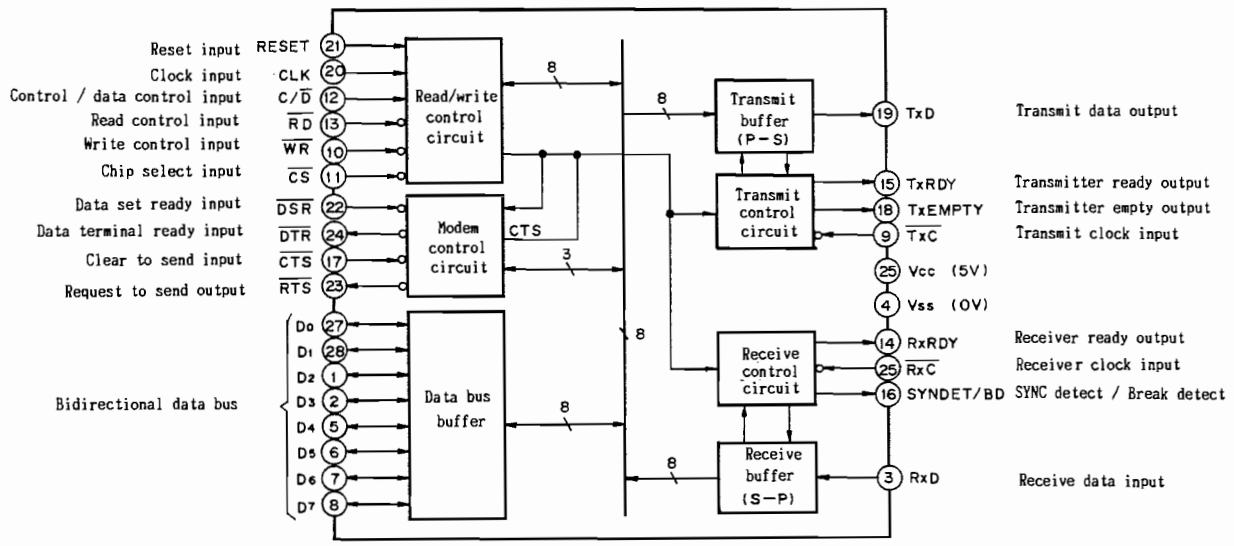
●Pin Connections (Top View)



●Pin Functions

No.	Symbol	Function
1	D_2	Bidirectional data bus
2	D_3	
3	RxD	Receive data input
4	V_{SS}	(0V)
5	D_4	Bidirectional data bus
6	D_5	
7	D_6	
8	D_7	
9	$\overline{TxC}$	Transmit clock input
10	$\overline{WR}$	Write control input
11	$\overline{CS}$	Chip select input
12	$C/\overline{D}$	Control / data control input
13	$\overline{RD}$	Read control input
14	RxRDY	Receiver ready input
15	TxRDY	Transmitter ready output
16	SYNDET/BD	SYNC detect / Break detect
17	$\overline{CTS}$	Clear to send input
18	TxEMPTY	Transmitter empty output
19	TxD	Transmit data output
20	CLK	Clock input
21	RESET	Reset input
22	$\overline{DSR}$	Data set ready input
23	$\overline{RTS}$	Request to send output
24	$\overline{DTR}$	Data terminal ready output
25	$\overline{RxC}$	Receive clock input
26	V_{CC}	(5V)
27	D_0	Bidirectional data bus
28	D_1	

●Block Diagram



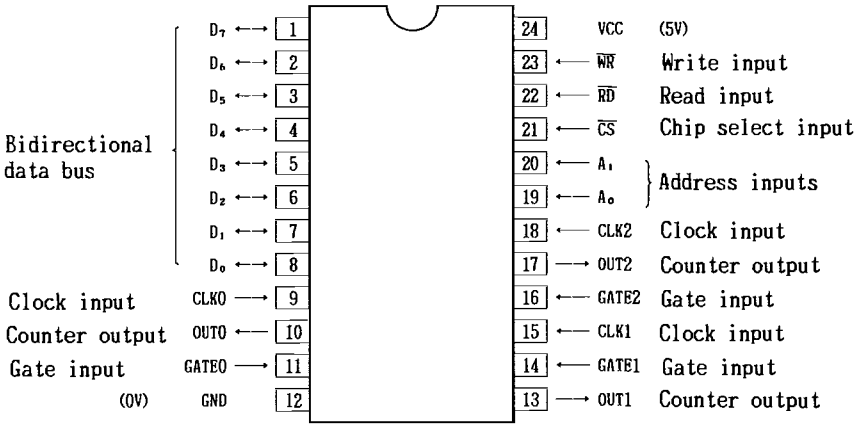
■M5L8253P-5 (IC130)

Programmable interval timer IC

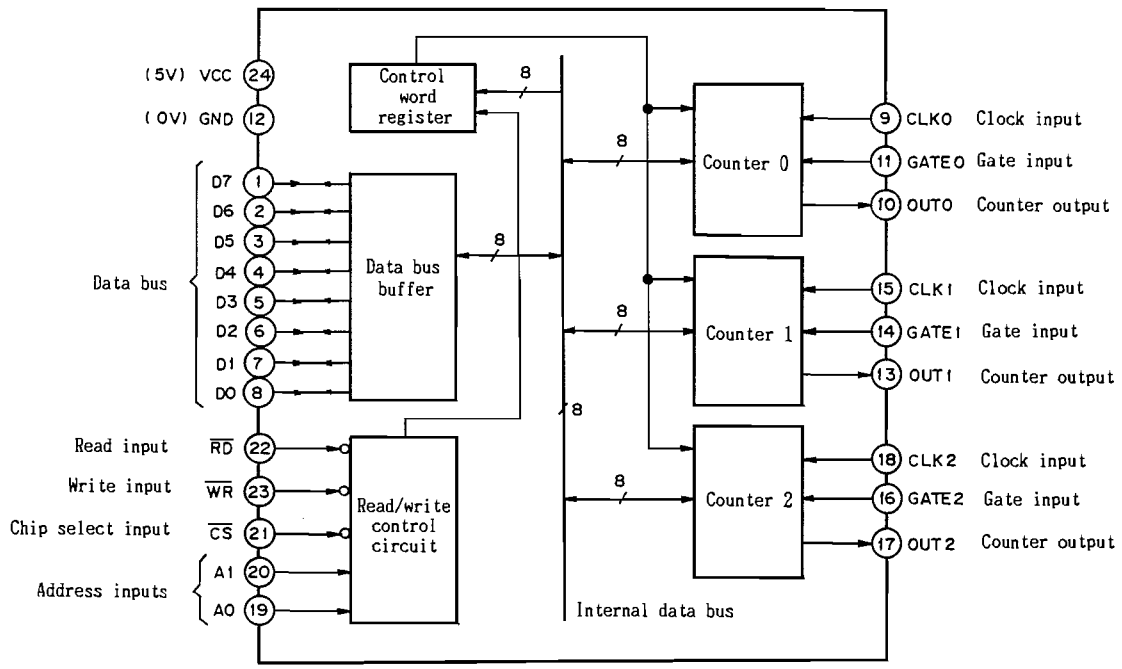
● Pin Functions

No.	Symbol	Function
1	D_7	Bidirectional data bus
2	D_6	
3	D_5	
4	D_4	
5	D_3	
6	D_2	
7	D_1	
8	D_0	
9	CLK 0	Clock input
10	OUT 0	Counter output
11	GATE 0	Gate input
12	GND	(0V)
13	OUT 1	Counter output
14	GATE 1	Gate input
15	CLK 1	Clock input
16	GATE 2	Gate input
17	OUT 2	Counter output
18	CLK 2	Clock input
19	A_0	Address input
20	A_1	
21	CS	Chip select input
22	RD	Read input
23	WR	Write input
24	V_{CC}	(5V)

● Pin Connections (Top View)



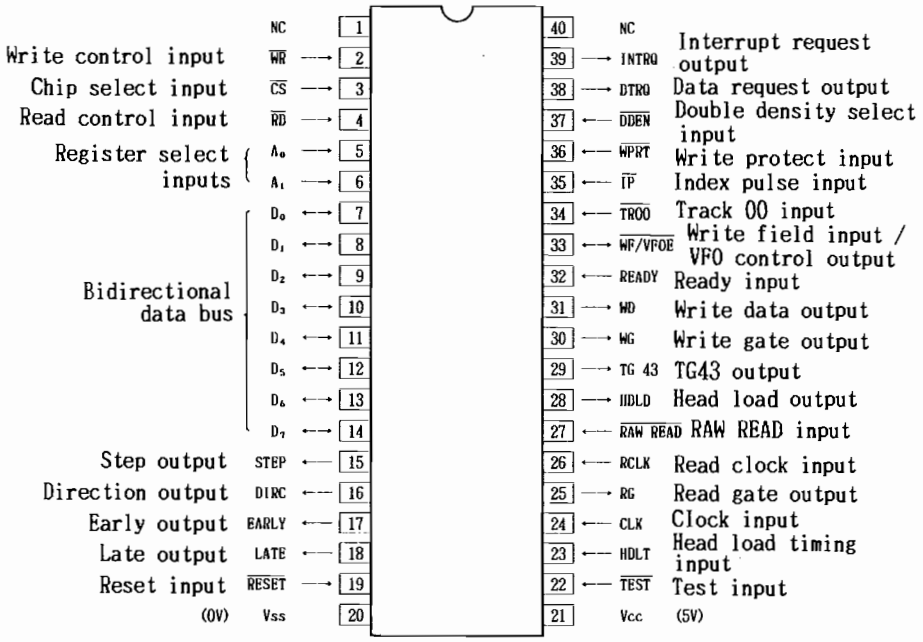
● Block Diagram



■M5W1793-02P (IC134)

Floppy disk control IC

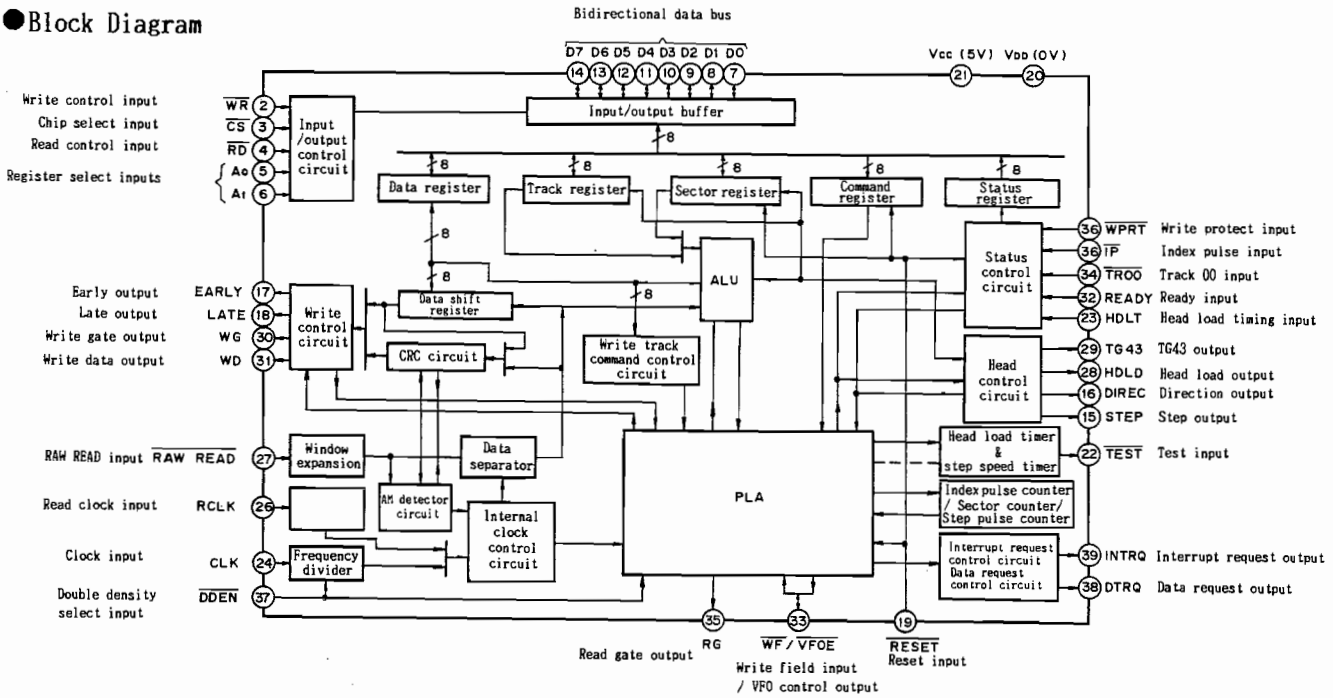
●Pin Connections (Top View)



●Pin Functions

No.	Symbol	Function
1	NC	Not connected
2	$\overline{WR}$	Write control input
3	$\overline{CS}$	Chip select input
4	$\overline{RD}$	Read control input
5	A_0	Register select inputs
6	A_1	
7	D_0	Bidirectional data bus
8	D_1	
9	D_2	
10	D_3	
11	D_4	
12	D_5	
13	D_6	
14	D_7	
15	STEP	Step output
16	DIRC	Direction output
17	EARLY	Early output
18	LATE	Late output
19	$\overline{RESET}$	Reset input
20	V_{SS}	0V
21	V_{CC}	5V
22	$\overline{TEST}$	Test input
23	HDLT	Head load timing input
24	CLK	Clock input
25	RG	Read gate output
26	RCLK	Read clock input
27	$\overline{RAW\ READ}$	RAW READ input
28	HDLD	Head load output
29	TG43	TG43 output
30	WG	Write gate output
31	WD	Write data output
32	READY	Ready input
33	$\overline{WF/VFOE}$	Write field input / VFO control output
34	$\overline{TR00}$	Track 00 input
35	$\overline{IP}$	Index pulse input
36	$\overline{WPRT}$	Write protect input
37	$\overline{DDEN}$	Double density select input
38	DTRQ	Data request output
39	INTRQ	Interrupt request output
40	NC	

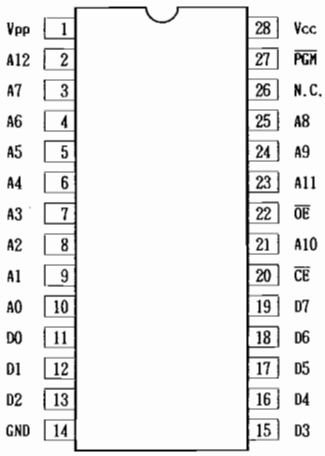
●Block Diagram



■M5L2764K-RS (IC114)

64K EP ROM (For RS-232C)

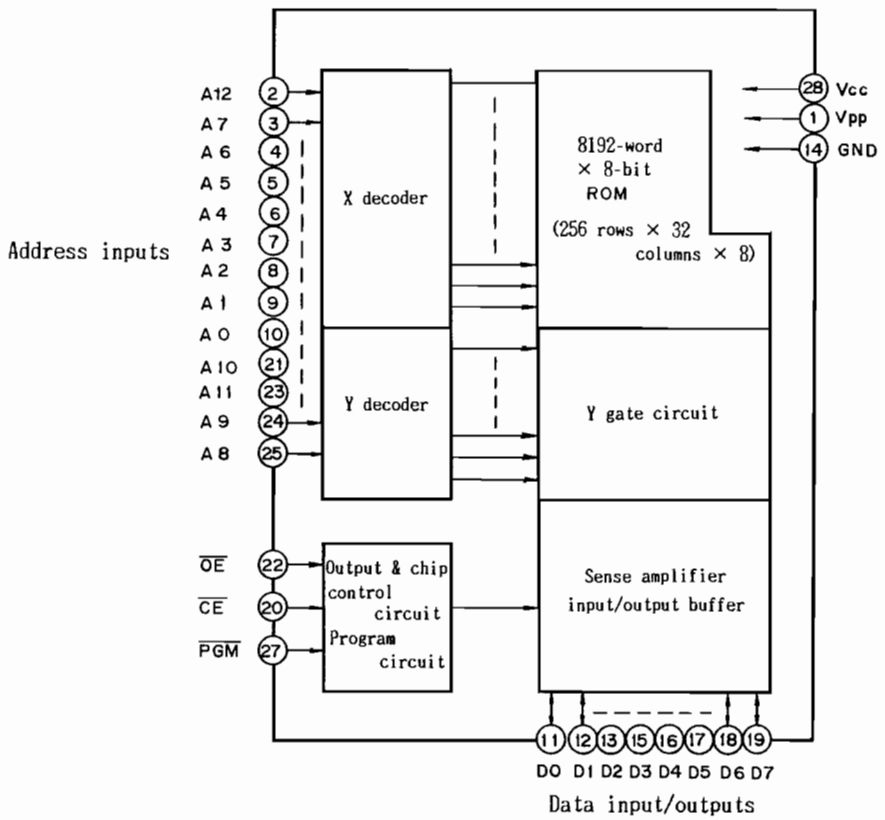
●Pin Connections (Top View)



●Pin Functions

No.	Symbol	Function	No.	Symbol	Function
1	V_{PP}	Program power supply (21V,5V)	15	D_3	Data input/outputs
2	A_{12}	Address inputs	16	D_4	
3	A_7		17	D_5	
4	A_6		18	D_6	
5	A_5		19	D_7	
6	A_4		20	$\overline{CE}$	Chip enable input
7	A_3		21	A_{10}	Address input
8	A_2		22	$\overline{OE}$	Output enable input
9	A_1		23	A_{11}	Address inputs
10	A_0		24	A_9	
11	D_0	Data input/outputs	25	A_8	
12	D_1		26	N.C.	
13	D_2		27	$\overline{PGM}$	Program pulse input
14	GND	0V	28	V_{CC}	5V

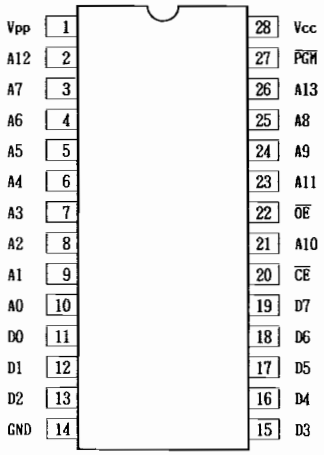
●Block Diagram



■M5L27128K-FD (IC113)

128K EP ROM (For floppy disk control)

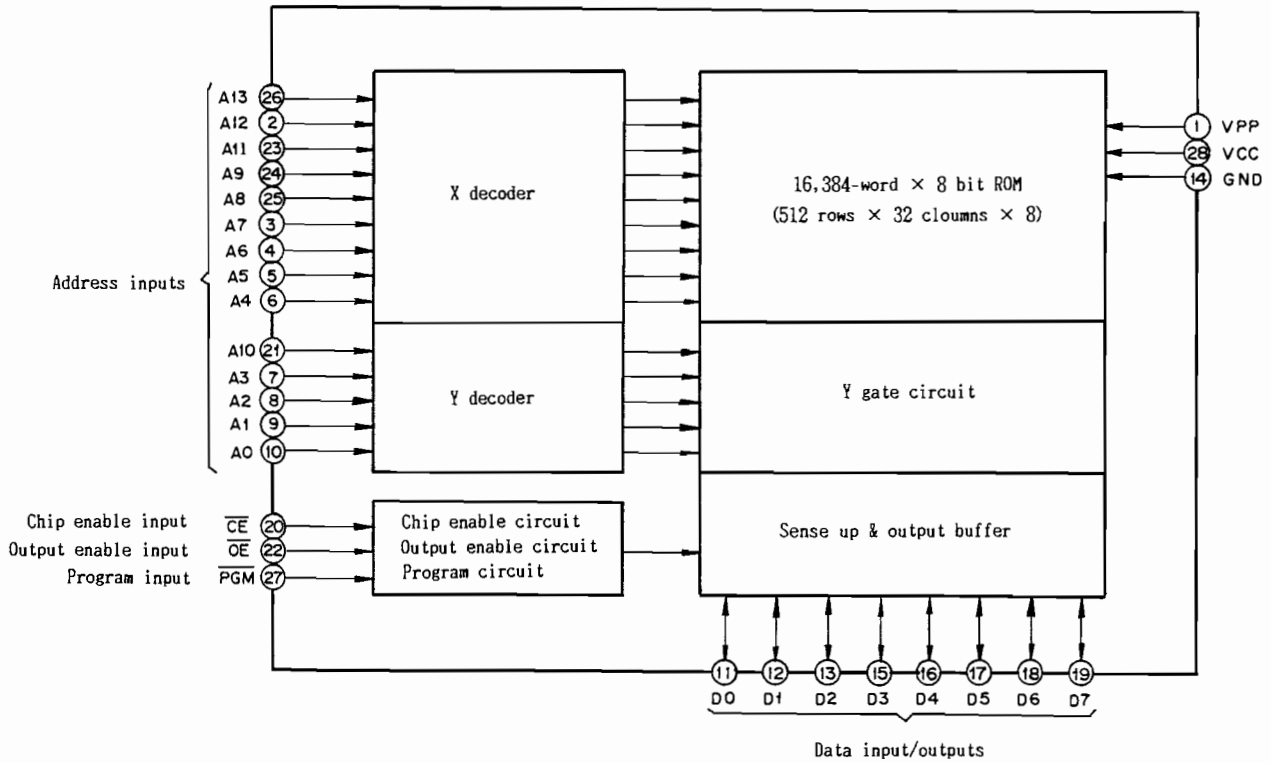
●Pin Connections (Top View)



●Pin Functions

No.	Symbol	Function	No.	Symbol	Function
1	V_{PP}	5V, 21V	15	D_3	Data input/outputs
2	A_{12}	Address inputs	16	D_4	
3	A_7		17	D_5	
4	A_6		18	D_6	
5	A_5		19	D_7	
6	A_4		20	$\overline{CE}$	Chip enable input
7	A_3		21	A_{10}	Address input
8	A_2		22	$\overline{OE}$	Output enable input
9	A_1		23	A_{11}	Address inputs
10	A_0		24	A_9	
11	D_0	Data input/outputs	25	A_8	
12	D_1		26	A_{13}	
13	D_2		27	$\overline{PGM}$	Program input
14	GND	0V	28	V_{CC}	5V

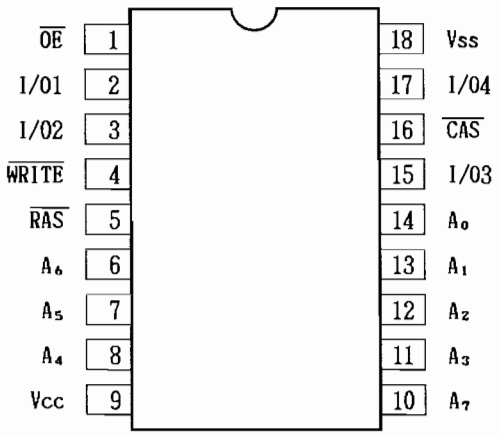
●Block Diagram



■MB81464-12 (IC109, 110, 125～128)

256K D RAM (120ns)

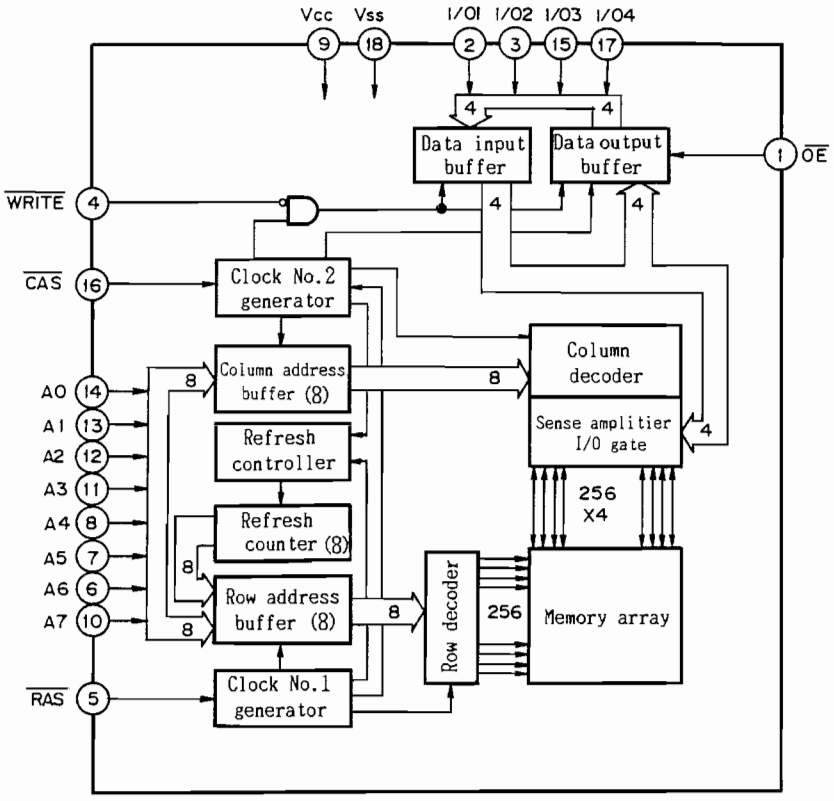
● Pin Connections (Top View)



● Pin Functions

No.	Symbol	Function
1	$\overline{OE}$	Output enable
2	I/O_1	Data input/outputs
3	I/O_2	
4	$\overline{WRITE}$	Read/write input
5	$\overline{RAS}$	Row address strobe
6	A_6	Address inputs
7	A_5	
8	A_4	
9	V_{CC}	
10	A_7	Address input
11	A_3	
12	A_2	
13	A_1	
14	A_0	
15	I/O_3	data input/output
16	$\overline{CAS}$	Column address strobe
17	I/O_4	Data input/output
18	V_{SS}	Ground

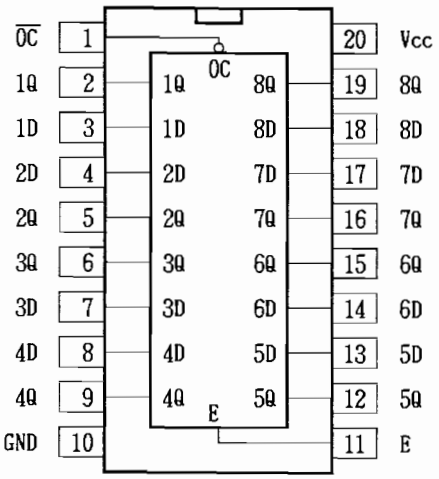
● Block Diagram



■M74LS373P (IC121)

LS TTL (D latch)

● Pin Connections (Top View)



● Function Table

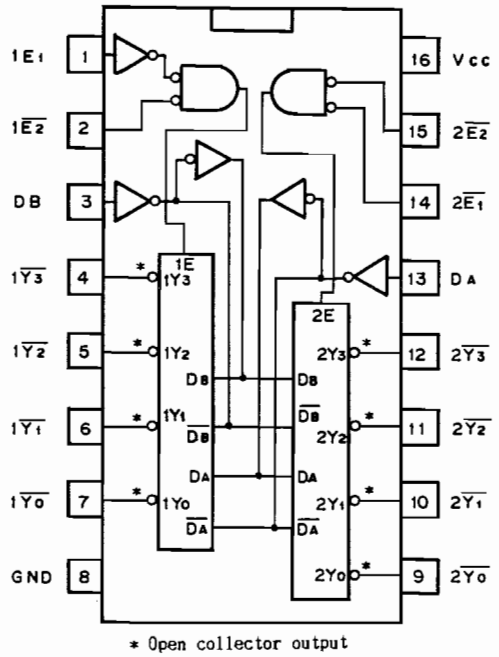
INPUT			OUTPUT
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q°
H	X	X	Z

Note Q°: Denotes output status before input conditions are set.
X : Either "H" or "L".
Z : High impedance status.

■M74LS156P (IC122, 123)

LS TTL (Decoder)

●Pin Connections (Top View)



* Open collector output

●Function Table

• 2-bit binary to 4-line decoder / 1-line to 4-line demultiplexer.

D_B	D_A	$1\overline{E_2}$	$1E_1$	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	$1\overline{Y_3}$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

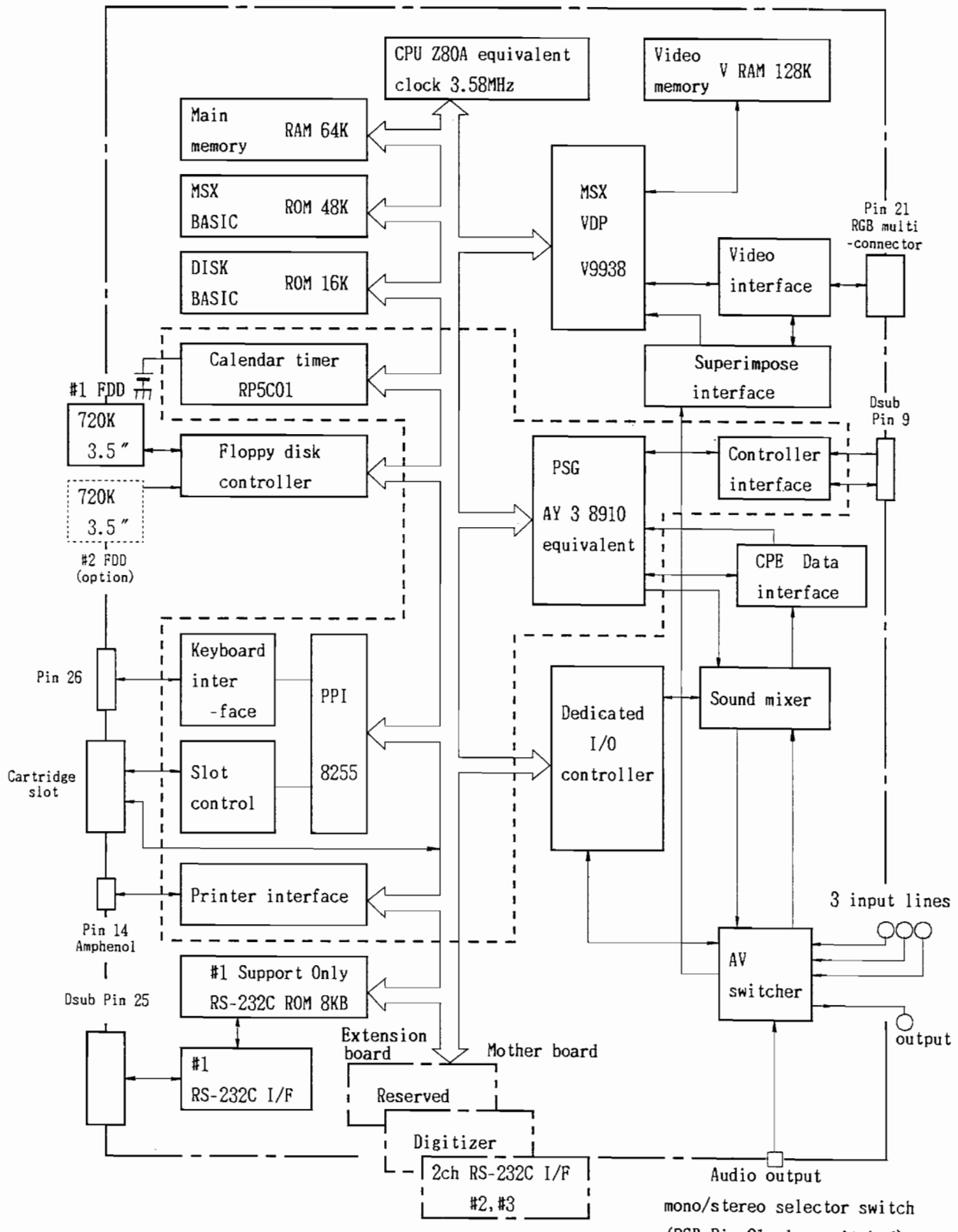
D_B	D_A	$2\overline{E_2}$	$2\overline{E_1}$	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Note X : Either "H" or "L".
Dc: Pin connected to $1E_1$ and $2\overline{E_1}$.
$\overline{E}$: Pin connected to $1\overline{E_2}$ and $2\overline{E_2}$.

• 3-bit binary to 8-line decoder / 1-line to 8-line demultiplexer.

D_C	D_B	D_A	$\overline{E}$	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	$1\overline{Y_3}$
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

8. BLOCK DIAGRAM



Note 1. Functions enclosed in [ ] are integrated on LSI S1985.

2. Extension board, and #2 FDD are optional.

9. CIRCUIT DESCRIPTION

9.1 Digital Section

In a system based on MSX_2 standard specifications and configured mainly for LD control purposes, the UC-V102 includes extension functions to enable the system to be used for a wide range of purposc and further increase the system's augmentability.

The following digital section circuits are described in this manual.

(1) Digital section block diagram
(2) Memory map and extension status
(3) I/O map
(4) RS-232C I/F
(5) Floppy disk
(6) Keyboard I/F
(7) Printer I/F
(8) Extension slots

9.1.1 Digital Section Block Diagram

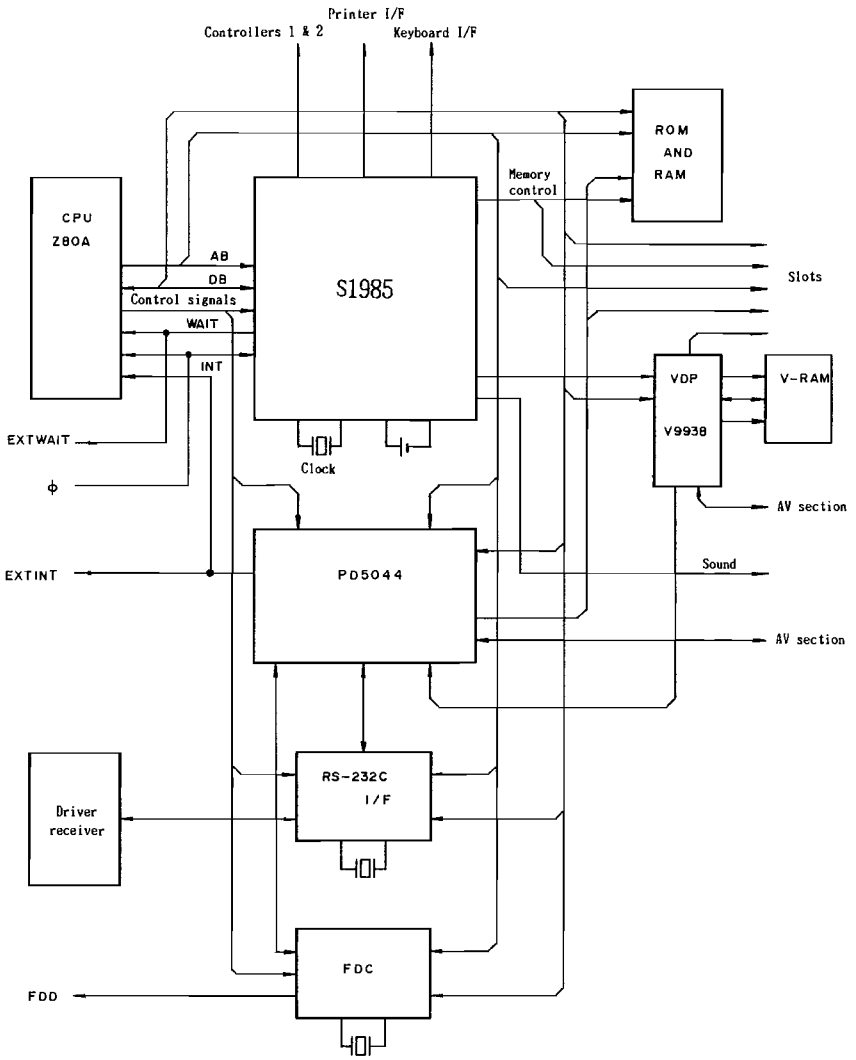


Fig. 9-1 Digital section block diagram

9.1.2 Memory Map and Extension Status

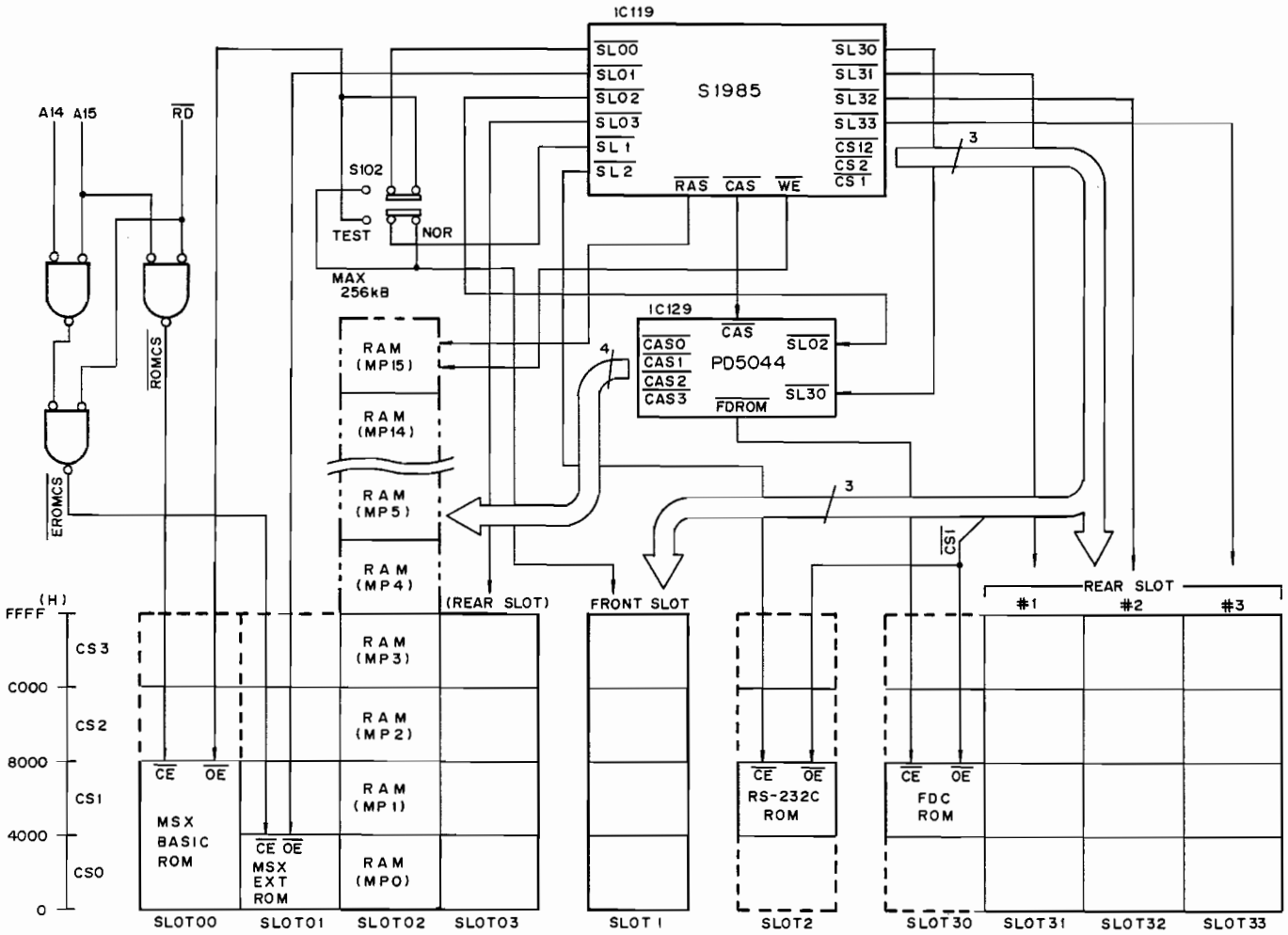


Fig. 9-2 Memory Map and Extension Status

9.1.3 I/O Map

00H-3FH	Reserved
50H	A/V SW 0 RGB multi-connector 1 INPUT 1 2 INPUT 2 3 INPUT 3
80H-87H	For RS-232C
80H	8251 Data
81H	8251 Status/command
82H	Status read / interrupt mask
83H	Not used
84H	8253
85H	8253
86H	8253
87H	8253
90H-91H	Printer port
90H	Bit 0 : Strobe output (write) Bit 1 : Status input (read)
91H	Print data
98H-9BH	VDP (V9938)
98H	VRAM access
99H	Command register access
9AH	Pallet register access (write only)
9BH	Indirect register designation (write only)
A0H-A2H	Sound generator (PSG)
A0H	Address latch
A1H	Data read
A2H	Data write
A8H-ABH	Parallel port (PPI)
A8H	Port A
A9H	Port B
AAH	Port C
ABH	Mode set
B4H-B5H	CLOCK
B4H	Address latch
B5H	Data
(D0H-D7H)	Floppy disk controller (FDC) The floppy disk controller includes a function designed to switch the floppy disk off by external signal. This function which can only be used while the FDC is accessed enables the system handle several different FDC interfaces.
D8H-D9H	Reserved for Kanji Rom
D8H	
D9H	
F5H	System control (write only) I/O device enabled when this bit is set to 1.
b0	(Reserved for kanji ROM)
b3	Superimpose (F7H read: Video input detect)
b5	RS-232C
F7H	A/V control
b0	Audio R L: Mixing ON (write)
b1	Audio L L: Mixing ON (write)
b2	——— : ———
b3	Video input detect L: No input (read)
b4	AV control L: TV (write)
b5	Ym control L: FULL TONE (write)
b6	VDP register 9 bit 4 inverted (write)
b7	VDP register 9 bit 5 inverted (write)
FCH-FFH	Memory mapper

★ I/O addresses not included in this table are reserved addresses.

Table 9-1 I/O map

9.1.4 RS-232C Interface Functional Composition

The UC-V102 RS-232C interface supported by extended BASIC can be set to a maximum baud rate of 19,200 bps. The practical limit, however, is 4,800 bps. Data transferred (by SAVE, LOAD command) at higher baud rates can result in data drop-out.

The RS-232C interface consists of the Universal Synchronous / Asynchronous Receiver / Transmitter (USART) M5L8251AP and the Programmable Interval Timer (PIT) M5L8253P-5. The USART devices mainly converts parallel 8-bit CPU data to serial data, and the PIT device generates the requisite clocks synchronized with the baud rate.

With USART capable of setting independent transmitting and receiving data speeds, the PIT counter #1 output is used as the transmitter clock and the counter #0 output as the receiver clock.

The fundamental clock for these counters is obtained by dividing a 3.6864MHz crystal resonator output (IC141 pin 6) by half at the IC136 flip-flop. The block diagram is shown in Figure 9-3.

IC132 (M75188P) line driver generates an output voltage greater than +5V and less than -5V to be passed to the signal line.
At the RS-232C interface, input voltages greater than +3V corresponds to data 0, and input voltages below -3V (minus voltage) correspond to data 1.
IC133 is a line receiver used to convert input signals greater than +3V and less than -3V to TTL levels.

(1) List of Extended BASIC Statement Used in RS-232C Communications

The following MSX standards extended BASIC has been prepared to enable the use of communication functions by RS-232C. Although commands, statements, and functions are the same as in MSX-BASIC, and MSX-DISK-BASIC, the communication functions have been extended by differences in format and specifying method for RS-232C communication operations.

Extended Statements (Used with CALL Statement)

COMINI	Initialization of communication functions.
COMTERM	Switch to terminal mode.
COMDTR	ER signal ON/OFF switching.
COMBREAK	Break signal transmitted.
COMSTAT	Determine status of RS-232C port.
COM GOSUB	Set start line of interrupt routine from RS-232C port.
COMON	Enable interrupt from RS-232C port.
COMOFF	Disable interrupt from RS-232C port.
COMSTOP	Hold interrupt from RS-232C port.

Commands

SAVE	Transmit program.
LOAD	Receive program.
RUN	Receive and then execute program.
MERGE	Receive program and merge it with program in memory.

Statemants

OPEN	Open file for RS-232C.
CLOSE	Close RS-232C file.
PRINT#	Transmit numerical and character strings.
PRINT# USING	Transmit numerical and character strings in specified format.
INPUT#	Receive numerical and character strings, and substitute in variables.
LINE INPUT#	Receive numerical and character strings, and substitute in variables.

Functions

EOF	Determined whether the EOF code (&H1A) has been received or not.
INPUT$	Receive character string of at least 1 character.
LOC	Determine number of data bytes in receive buffer.
LOF	Determine remaining number of bytes in receive buffer.

Device no.

UC-V102 is equipped with one RS-232C port. The specified device no. is 0.

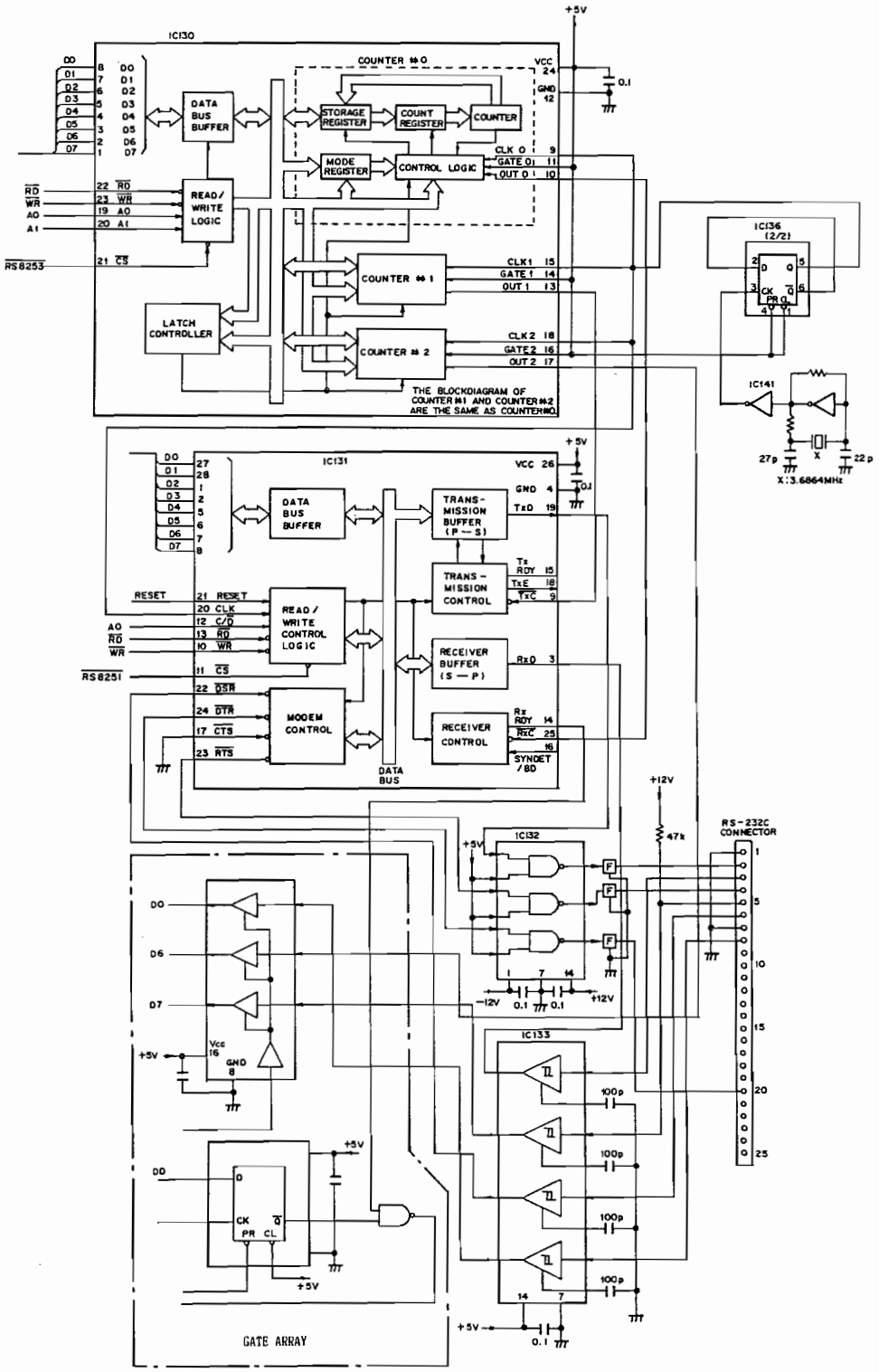


Fig. 9-3 RS-232C section block diagram

(2) Example of LD-V4200 Control in UC-V102

① Set all LD-V4200 function switches OFF (upper position). 4.8K bps, CR terminated.

② Key in the following control software.

```
 10  CALL COMINI ("8N1NHAAN",4800,4800,1)
 20  OPEN "COM:" AS #1
 30  INPUT CM$ : GOSUB 100
 40  PRINT ST$ : GOTO 30
100  PRINT#1,CM$ : INPUT#1,ST$ : RETURN
```

10: RS-232C port initialization
8-bit data, parity none, 1 stop bit
No Xon/off control
CS control ON : Check whether player power is on or not
Auto LF ON, SI/SO control OFF
Receive and transmit speeds 4800 bps
CS delay time 1 second

20: Open the RS-232C port

30: Key in and transmit command from key board

40: Display status

100: Basic access subroutine
Wait until status (ST$) is received after transmitting command before returning.

Command Commentary

Commands which can be executed by LD-V4200 are listed below.

	Command	Mnemonic	
1	DOOR OPEN		OP
2	REJECT		RJ
3	START		SA
4	PLAY	(address)	PL
5	PAUSE		PA
6	STILL		ST
7	STEP FORWARD		SF
8	STEP REVERSE		SR
9	SCAN FORWARD		NF
10	SCAN REVERSE		NR
11	MULTI-SPEED FORWARD	(address)	MF
12	MULTI-SPEED REVERSE	(address)	MR
13	SPEED	argument	SP
14	SEARCH	address	SE
15	STOP MARKER	address	SM
16	FRAME		FR
17	TIME		TM
18	CHAPTER		CH
19	AUDIO CONTROL	argument	AD
20	VIDEO CONTROL	argument	VD
21	DISPLAY CONTROL	argument	DS
22	CLEAR		CL
23	FRAME NUMBER REQUEST		?F
24	TIME CODE REQUEST		?T
25	CHAPTER NUMBER REQUEST		?C
26	PLAYER ACTIVE MODE REQUEST		?P
27	DISC STATUS REQUEST		?D
28	COMMUNICATION CONTROL	argument	CM
29	CCR MODE REQUEST		?M
30	LVP MODEL NAME REQUEST		?X
31	KEY LOCK	argument	KL
32	REG. A SET (DISPLAY)	argument	RA
33	REG. B SET (SQ CONT)	argument	RB
34	REG. C SET (MISCELLANY)	argument	RC
35	CLEAR SCREEN		CS
36	PRINT	argument	PR
37	LEAD OUT SYMBOL		LO

Table 9-2 Control commands

9.1.5 Floppy Disk

The standard UC-V102 configuration includes one 3.5 inch 2DD floppy disk drive capable of recording and reading programs and data in DISK BASIC. And MSX DOS can be started up by using an MSX DOS system disk.
Floppy disk operations and control procedures are described in this section.

(1) Diskette

The diskette recording medium consists of a thin circular film coated with magnetic material and housed in a hard plastic case. Both dual-sided (2DD) and single-sided (1DD) diskettes can be used in UC-V102.
The recording area of the diskette is divided into eccentric rings called tracks which are further divided into data blocks called sectors (the minimum recording unit). 2DD diskettes contain 80 tracks per side making a total of 160 tracks.
The configuration of a single track is outlined in Figure 9-4.

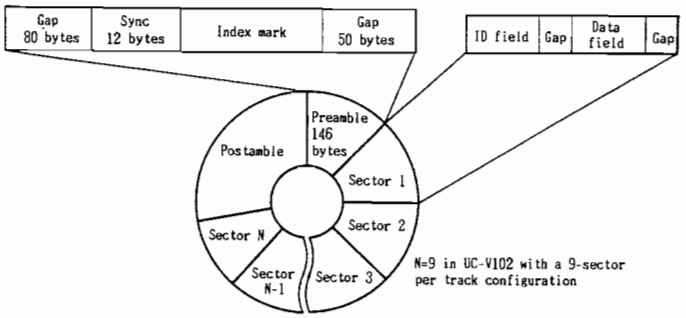


Fig. 9-4 Track configuration

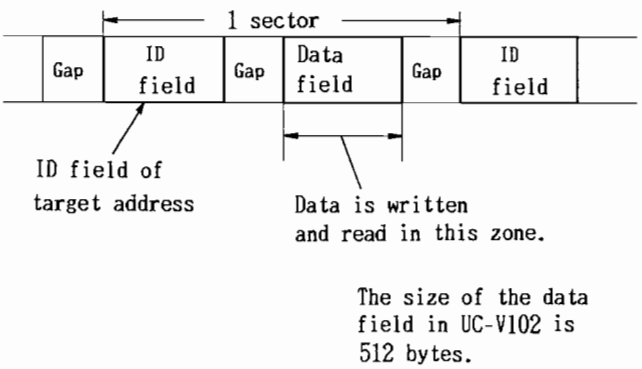


Fig. 9-5 Sector configuration

The sector is the smallest unit involved in recording and reading of data to and from floppy disks. All sector include an ID field where the same fixed data remains unchanged when ordinary data is recorded (written) and read. (The disk is said to be formatted when data is recorded in these ID fields.)
The data recorded in the ID field is shown in Table 9-3. Each sector is given its own unique number. No two sectors can have ID fields of the same value.
That is, floppy disk data is managed by side number (0 or 1), track number (0 thru 79), and sector number (1 thru 9), thereby enabling a single sector to be accessed.

Track number	0 thru 79 (The outermost track is number 0)
Side number	0 or 1 (The under side is 0)
Sector number	1 thru 9 (Numbered in sequence from INDEX)

Table 9-3 Sector ID field contents

The recording capacity of a 2DD disk can be calculated from the above values.

512 bytes/sector × 9 sectors/track
× 80 tracks/side × 2 sides = 737,280 bytes

Since track 0 is not used for ordinary data, the number of tracks available is 79, making a total of 728,064 bytes. The nominal rating is 720K bytes (or 360K bytes for 1DD disks).

(2) MFM modulated data recording method

Data can be recorded by either FM modulation or MFM modulation. The MFM method has a recording density twice that of the FM method. The bit patterns used in the two methods are shown in Figure 9-6. The writing data frequency in the MFM method is about half the frequency in the FM method when the same data is recorded. That is, twice the amount of data can be recorded when recording on identical media.

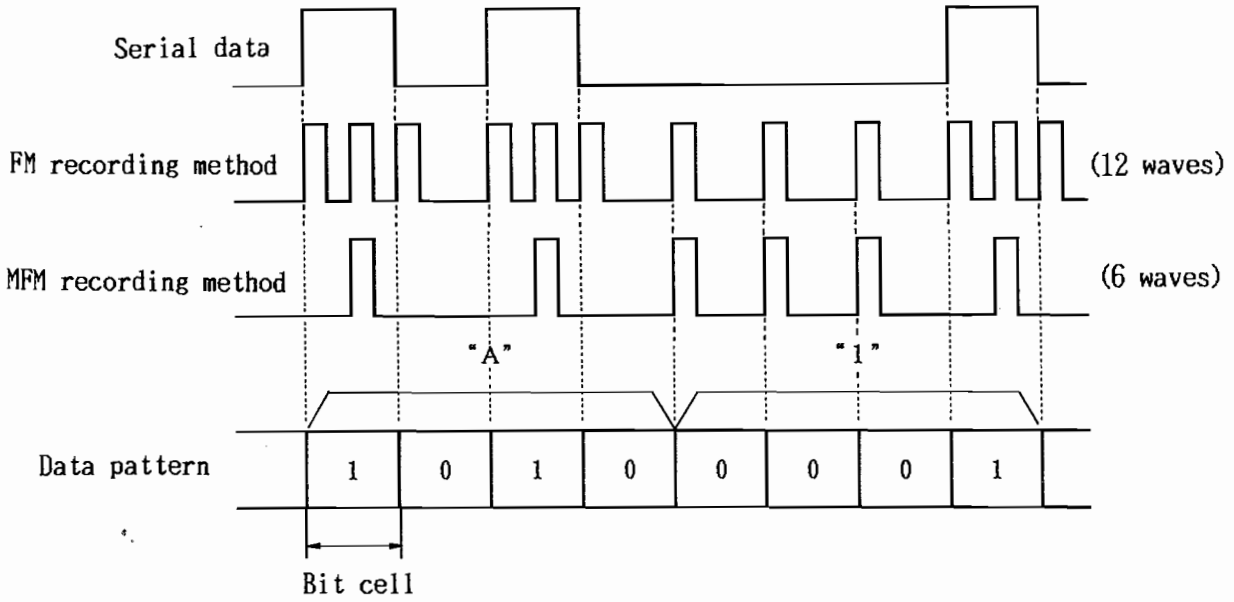


Fig. 9-6 FM and MFM recording method bit patterns

(3) Reproduction of Read data/VFO circuit

When the MFM modulation method is used, data is recorded on the diskette as pulse signals. And when these pulse signals are retrieved during data reading, a data window signal (see Figure 9-8) is generated to reproduce the data from the pulse train. The data is reproduced as 0 or 1 depending on whether a pulse is read or not at the data window signal.

These window signals are generated by the VFO circuit in the SED9421 IC which includes a PLL circuit block outlined in Figure 9-7. Data window and data pulse signals are obtained from the data read from the floppy disk, and are passed to the floppy disk controller (FDC) in M5W1793.

The PLL circuit is locked during the SYNC byte interval (12 successive bytes of "00" data) included in each sector, thereby generating a window signal during sector reading.

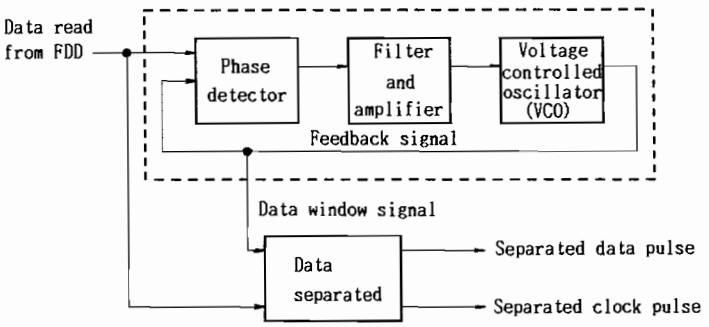


Fig. 9-7 VFO circuit block diagram

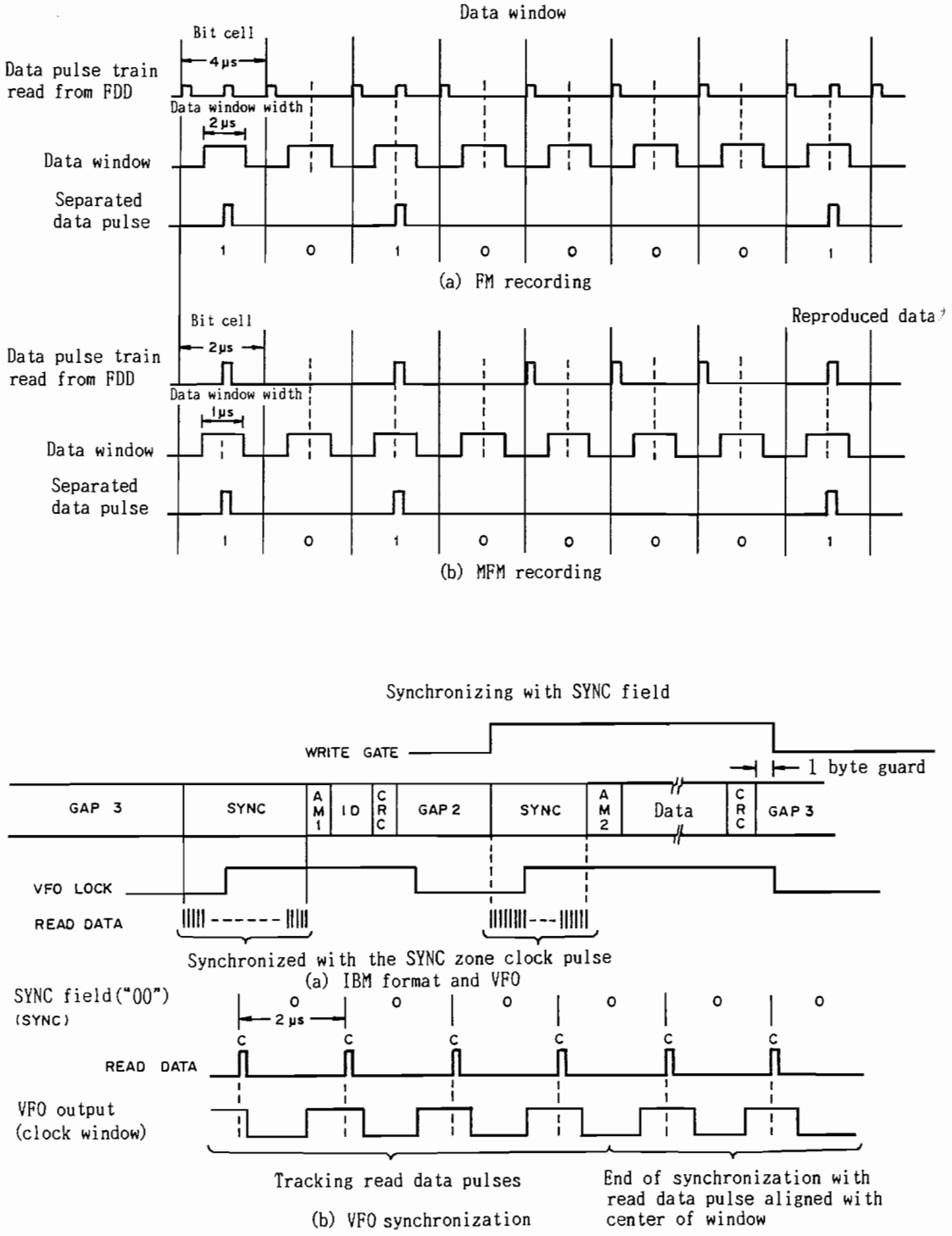


Fig. 9-8 Data window signal timing chart

(4) Floppy disk drive control

To enable random access of data recorded on diskette, the floppy disk drive head must be controlled. And each track, side, and sector must be designated.
Designated track, side and sector are set by control signals passed from the floppy disk controller (FDC) to the floppy disk drive (FDD).

Tracks are specified by STEP and DIRC signals used to shift the head. The head is shifted one track at a time by each STEP signal, and the direction (towards the center or the outer edge of the disk) is specified by the DIRC signal. The side is specified switching bit 0 of the register at address 7FFCH - side 0 (reverse) if the bit is 0, and side 1 (face) if the bit is 1.
The ID field data of each sector is read, and when data which matches the specified sector number is located, that data is read/written from to that sector.

(5) Interface

The interface between the floppy disk drive and floppy disk controller is all negative logic, and all drive operations are executed by open collector. This enables more than one floppy disk drive to be connected.

(6) FDC operation clock

The IC135 (SED9421C0B) VFO IC incorporates a built-in FDC clock generator. A 1MHz clock obtained by dividing the fundamental frequency of 16MHz is supplied as the clock from the ϕ_Z pin (15).

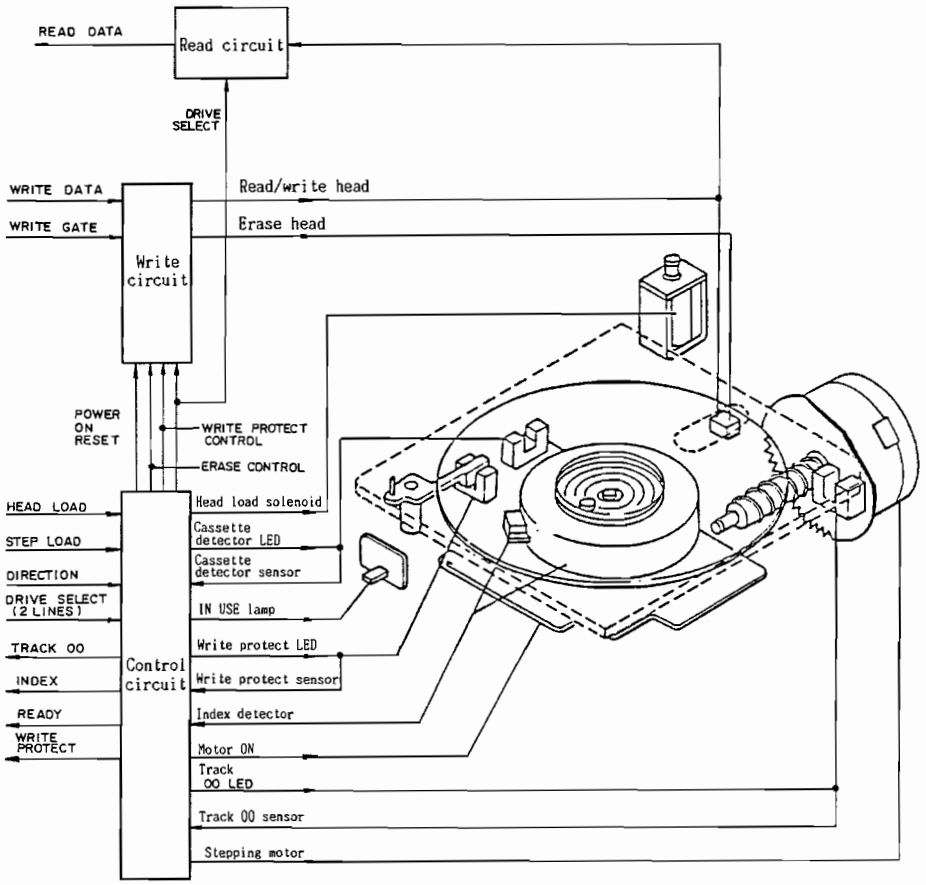


Fig. 9-9 Basic floppy disk construction

(7) Reference : Floppy disk drive specifications

The 3.5 inch 2DD (2 sided double-density double track) type floppy disk drive handles 1M bytes on unformatted disks and 720K bytes on formatted disks.

Major specifications are listed below.

	Double density
Recording capacity	
Unformatted	1000K bytes
Disk	1000K bytes
Side	500K bytes
Track	6.25K bytes
Transfer rate	250K bit/sec.
Rotation delay (average)	100msec.
Access times	
Track to track	3msec.
Average	94msec. (including step time of 3msec. and settling time)
Settling time	15msec.
Motor start time	400msec. (max. 700msec. up to READY output)

	Double density
Recording density	8717BPI
Magnetic flux inversion dendity	8717FCI
Recording modulation	MFM
Track density	135TPI
No. of cylinders	80
No. of tracks	160
No. of heads	2
Rotational speed	300RPM
Rotation period	200msec.
Index	1
Medium	3.5 inch micro flexible disk cartridge

Table 9-4 Floppy disk specifications

● Functional Composition

1. General Operation

The MF353AF floppy disk drive consists of a media drive mechanism, two read/write heads, an actuator which positions the heads at the read/write track, and a number of electrical circuits involved in driving these mechanisms.

When a diskette is inserted, the media drive mechanism clamps the diskette onto a spindle coupled directly to a DC brushless direct-drive motor and rotates it at 300 rpm. The positioning actuator moves the read/write head to the desired track, and the head proceeds to read or write data at that track.

2. Electrical Circuits

The electrical circuits used to drive the various stages are mounted on a single PCB. These circuits include :

- Line driver and receiver for transfer of signals with the host system.
- Drive selector.
- Index detector.
- Head positioning actuator drive circuit.
- Spindle motor control circuit.
- Read/write circuit.
- Write protect circuit.
- Track 00 detector.
- Drive READY detector.
- Head selector.
- IN USE and panel indicator LED drive circuit.

A motor drive circuit and speed detector are mounted on the spindle motor PCB together with a Hall element detector.

3. Rotation Drive Mechanism

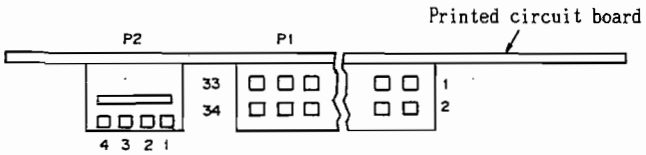
The disk cartridge drive mechanism turns the disk at 300 rpm via a spindle directly coupled to a DC brushless direct-drive motor.

4. Positioning Mechanism

The read/write head is positioned in the following manner.

The carriage assembly unit is connected in a read screw groove section of the stepping motor output axis. Each time the stepping motor turns through 15° , the read/write head is shifted by one track in the specified direction.

Electric Interface



P1/P2 connector

Line voltage	Pin no.	Remarks
+12V DC	1	
+12V DC Return	2	
+5V DC Return	3	
+5V DC	4	

Fig. 9-10 Connector layout and function table

Signal name	Signal pin no.	GND return pin no.	Input/output
SPARE	2	1	—
IN USE	4	3	Input
DRIVE SELECT 3	6	5	Input
INDEX	8	7	Output
DRIVE SELECT 0	10	9	Input
DRIVE SELECT 1	12	11	Input
DRIVE SELECT 2	14	13	Input
MOTOR ON	16	15	Input
DIRECTION SELECT	18	17	Input
STEP	20	19	Input
WRITE DATA	22	21	Input
WRITE GATE	24	23	Input
TRACK 00	26	25	Output
WRITE PROTECT	28	27	Output
READ DATA	30	29	Output
SIDE ONE SELECT	32	31	Input
READY	34	33	Output

Table 9-5 Function table

5. Input Signal Line

Eleven input signal lines are connected to the drive. These signal lines are divided into two groups - one consisting of signals multiplexed in multi-drive systems, and the other consisting of the multiplexing signals. The four multiplexing signals are listed below.

- ●DRIVE SELECT 0
- ●DRIVE SELECT 1
- ●DRIVE SELECT 2
- ●DRIVE SELECT 3

(1) DRIVE SELECT 0 THRU 3

When the DRIVE SELECT line is at logical "0" level, the multiplexed I/O line is activated and read/write is enabled. These four isolated input signal line DRIVE SELECT 0 thru 3 have been incorporated to permit reciprocal multplexing with four drives connected to the one system. The PCB mounted short plugs DS0 thru DS3 are connected to the respective DRIVE SELECT lines and are used to activate the corresponding drives.

(2) SIDE ONE SELECT

This interface line is used to select side 0 or 1 (of a 2 sided diskette) for reading or writing. The side 1 head is selected when the line is logical "1", and the side 0 head is selected when the line is logical "0".

(3) DIRECTION SELECT

The direction in which the read/write head is shifted when a step signal pulse is applied is controlled by this line interface signal.
The read/write head is shifted towards the outer edge of the disk when the signal is logical "1", and towards the center when logical "0".

(4) STEP

The STEP interface line pulse signal shifts the read/write head in the direction defined by the DIRECTION SELECT line. The head is shifted one track for each signal pulse applied to the step line.
With this line normally at logical "1" level, step operation is commenced by the trailing edge of a "negative going pulse" (level inverted from logical "0" to logical "1").

(5) WRITE GATE

The write driver is activated when this interface line is changed to logical "0". Data passed to the write data line for the selected side is then recorded on that side of the diskette. When the line is reverted to logical "1", the write driver becomes inactive, and the read data logic is enabled.

(6) WRITE DATA

Data to be recorded on the diskette is passed to this interface line. With this line normally logical "1", the write current is inverted by the leading edge (level inverted from logical "1" to logical "0") of a data pulse (negative going pulse), and data bits are then written to the diskette. This line is enabled when the write gate is logical "0".

(7) IN USE

The front panel IN USE indicator LED comes on when this interface line becomes logical "0". This LED is also switched on by DRIVE SELECT.

(8) MOTOR ON

The spindle motor is started when the MOTOR ON interface line becomes logical "0".

6. Output Signal Line

(1) INDEX

With this interface line normally at logical "1", a single logical "0" output pulse (approx. 4.0msec pulse width) is generated during each revolution of the diskette (cycle period of 200msec.). This output signal indicates the track start while the diskette is rotating.

(2) TRACK 00

When at logical "0", this interface line indicates that the read/write head is positioned at track 00. And when the selected drive output is logical "1", the read/write head is positioned at any other track except track 00.

(3) READY

The READY interface line becomes logical "1" when the spindle motor is stopped, or when no diskette is detected in the drive. When a diskette is inserted, an index pulse is detected, power is supplied to the DC supply lines (+5V and +12V), and the READY interface line becomes logical "0" after three index pulses are detected.

(4) READ DATA

Data recorded on the diskette is read by the read/write head, and converted to a pulse signal in the electrical circuits. The resultant RAW DATA output (consisting of combined clock and data) is passed to this READ DATA interface line. This interface line is normally logical "1". A logical "0" output pulse (negative going pulse) is generated when data is read.

(5) WRITE PROTECT

The WRITE PROTECT interface line is used to alert the host system when a write-protected diskette is inserted. The line becomes logical "0" when such a diskette is inserted, and write operations are inhibited irregardless of whether the WRITE GATE line becomes active.

7. Short Plugs

1) Drive select conditions

DS0 thru DS3

When more than one drive is connected to the system, the shorting plug is plugged into DS0 thru DS3 to select the corresponding drive, and enable transfer of input/output signals only with drives where the DRIVE SELECT line is logical "0".

If, for example, the DRIVE SELECT 0 line of the drive where DS0 is shorted is logical "0", that drive is selected.

UC-V102 has been designed to accommodate a second drive. When a second drive is installed, a short plug must be set at the position marked DS1 on the circuit board.

If the DS0 shorting plug is set, the two drive outputs will collide and the system will not function properly.

8. Signal Interfacing

Signal interfacing is divided into control signal and data signal interfacing. Note that all interface signal lines are TTL level.
The signal levels and characteristics are summarized below.

- True = logical "0" = V_L 0V TO +0.4V
  Iin max. 40mA
- False = logical "1" = V_H 0V + 3.8V TO +5.25V
  Iin 0mA
- INPUT IMPEDANCE = 1k OHM

9.1.6 Keyboard I/F

Ra is the current control resistor, Rb and Rc are the IC122 and IC123 pull-up resistor, and F is an EMI filter.

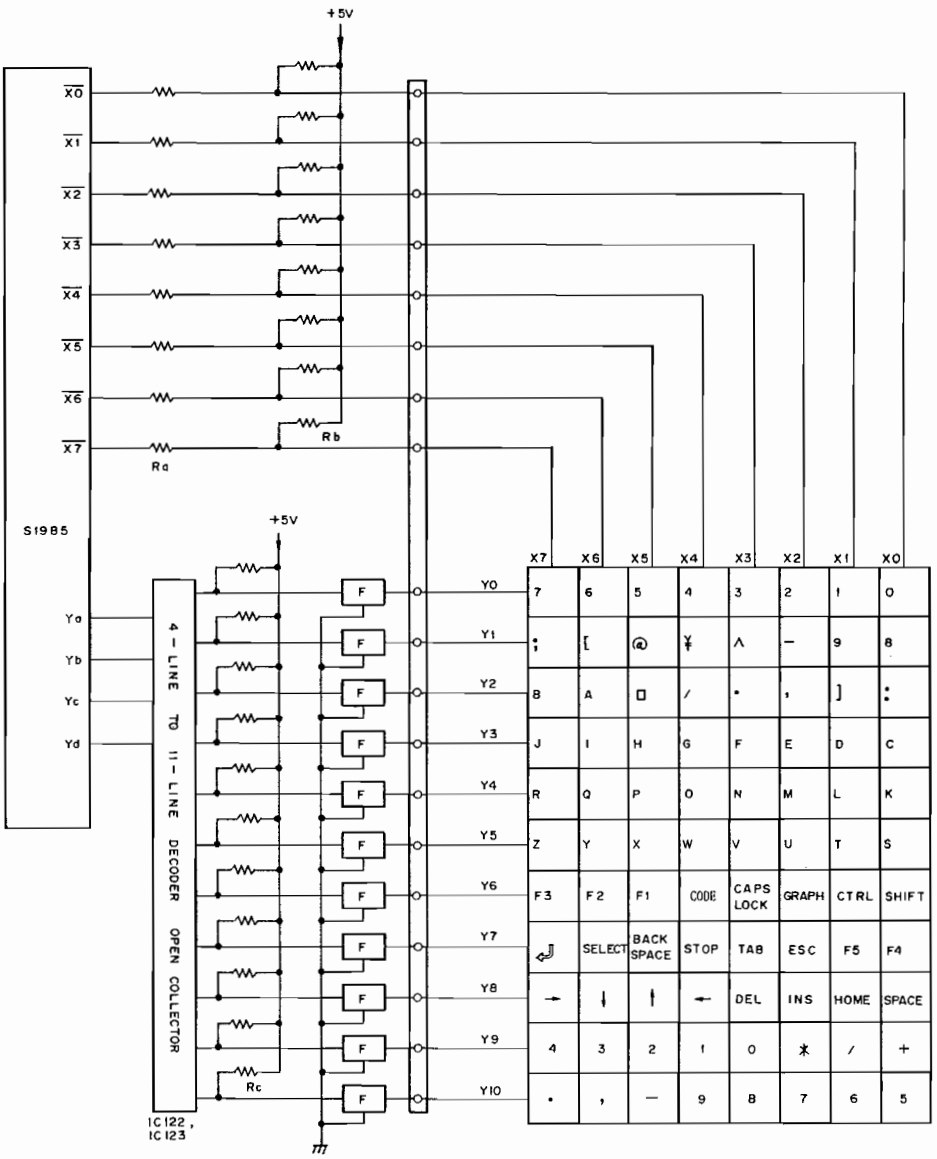


Fig. 9-11 Key board I/F block diagram

9.1.7 Printer I/F

PBUSY: When an input signal is read to the PBUSY pin, an output of the same level (as the input level) appears at B1.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	R								

$\overline{PSTB}$: If B0 is writen as "0", the $\overline{PSTB}$ pin becomes "0" when the WR signal returns to "1". And if B0 is subsequently written as "1", the $\overline{PSTB}$ signal returns to "1".

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	W								

PWR: If data is written when output status is set by PDIR "1", a positive PWR output signal which conforms with the $\overline{WR}$ signal pulse width is obtained at the PWR pin. External circuitry latches the data when this signal returns to "0" and passes the data to the output. If input status is then set by PDIR "0", the PWR pin stays at "1", and also maintains that level if output status is set again. The pin is returned to "0" after accessing of 91(H) has been completed.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
91 (H)	W	Data							

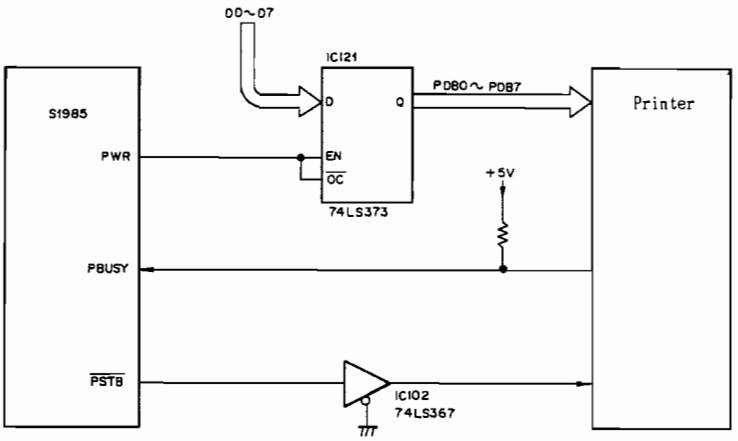


Fig. 9-12 Printer I/F block diagram

9.1.8 Extension Slots

UC-V102 is equipped with extension slots in the rear panel capable of accommodating up to three extension cards. Mounting additional boards such as extension RS-232C and digitizer boards expands the functions of the system.

- Major signal lines
  - CPU data bus
  - CPU address bus
  - CPU control lines
  - V9938 color bus
  - External composite video
  - External composite sync
  - V9938 DHCLK (10.74MHz)
  - V9938 DLCLK (5.37MHz)
  - Slot select signal
  - Chip select signal
  - Mapper address (MA14 thru MA17)
  - RAM control signals
- Power supplies
  - +5V
  - +12V
  - −12V

9.2 AV Section

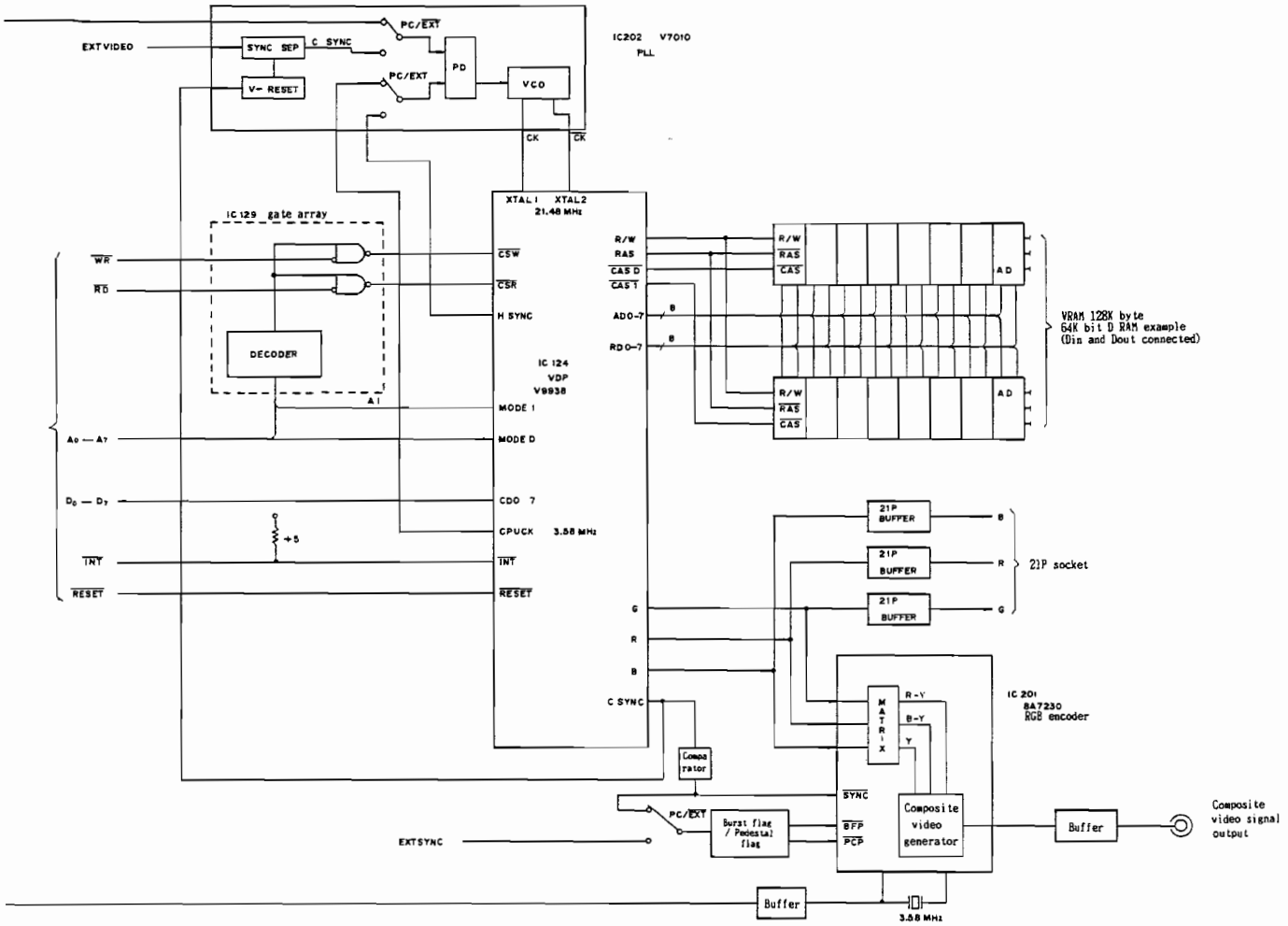


Fig. 9-13 AV video section block diagram

9.2.1 PLL SYNC SEP (V7010)

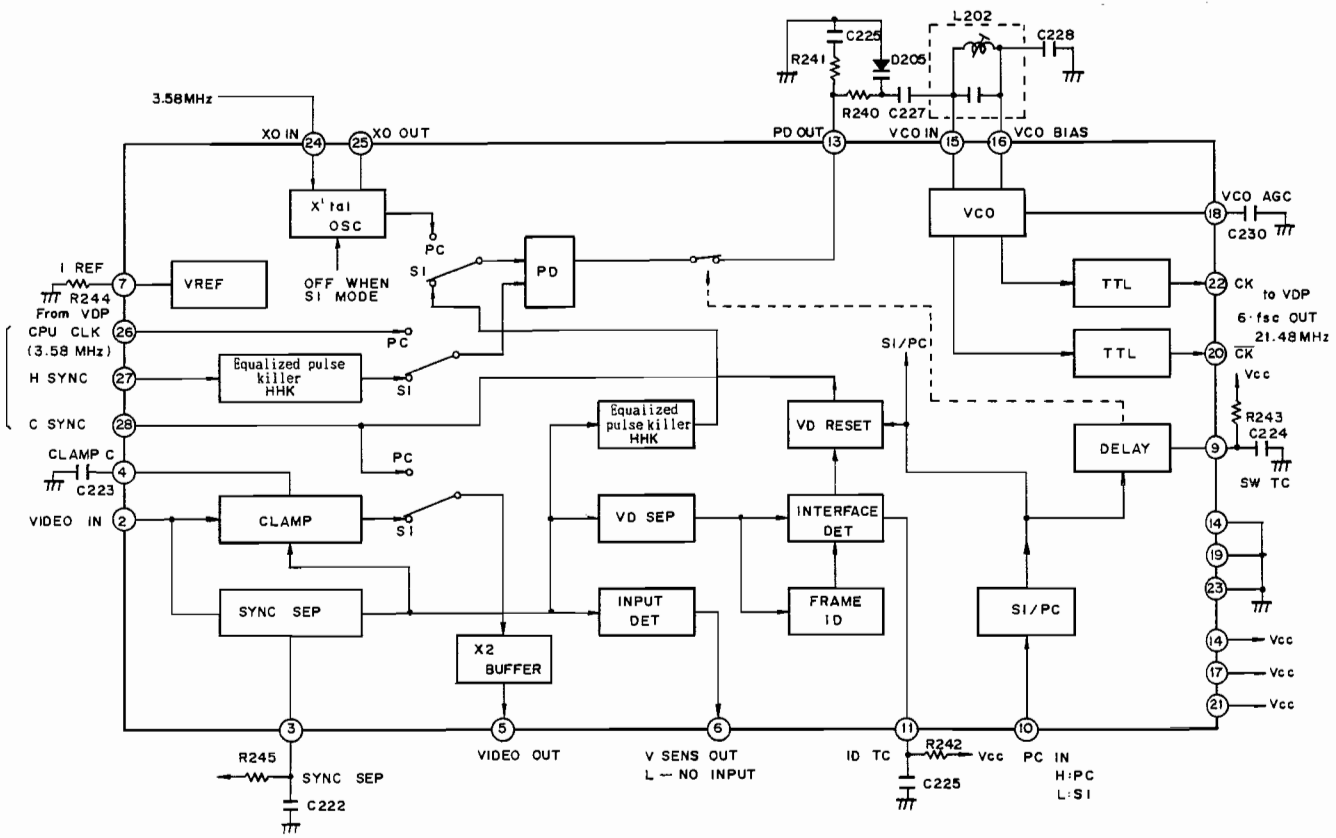


Fig. 9-14 IC202 (V7010) block diagram

(1) Internal synchronization

A 3.58MHz signal from X201 (XTAL) is passed via buffer Q212 to pin 24 of IC202, and each switch is set to PC when pin 10 is at H level. The phase of the pin 24 3.58MHz input is compared with the phase of a 3.58MHz input signal from VDP applied to pin 26. The comparison result output is generated using pin 24 of XO_{IN} as a reference.

A control voltage is passed via a low pass filter (R241 & C225) to a variable capacitance diode D205. (Together with L202 and C227, D205 forms a 21.48Hz tank circuit.) the VCO output is converted to TTL level via a buffer, and is passed to VDP as CK and inverted phase $\overline{CK}$. This CK is divded by 6 in the VDP to obtain the 3.58MHz signal which is passed to IC202. A composite synchronizing signal from VDP is passed via a 6dB buffer to the Video Out pin (pin 5).

(2) External synchronization

The synchronizing signal in the composite video signal applied to the VIDEO IN pin of IC202 (pin 2) is separated (SYNC SEP). And from this the vertical synchronizing signal is separated (VD SEP). If the video signal is interlaced, an external synchronizing reset signal is passed to VDP in field 1.

Pin 6 is at H level (video present) while the composite video signal is applied to pin 2, but at L level (no video) while no input is applied.

The switch is in the SI (external synchronization) position when pin 10 is at L level. The external composite synchronizing signal separated from the video signal on pin 2 and the Hsync input applied to pin 27 from VDP is passed via HHK (equalized pulse killer) with the resultant phase being compared with the original external composite synchronizing signal.

The composite video signal applied to pin 2 is passed to pin 5 via a 6dB buffer.

9.2.2 GENLOCK Method

The GENLOCK method compares the phase of the MSX-VIDEO HSYNC output and external HSYNC with negative feedback being applied to the system clock. Jitter is not generated by this method.

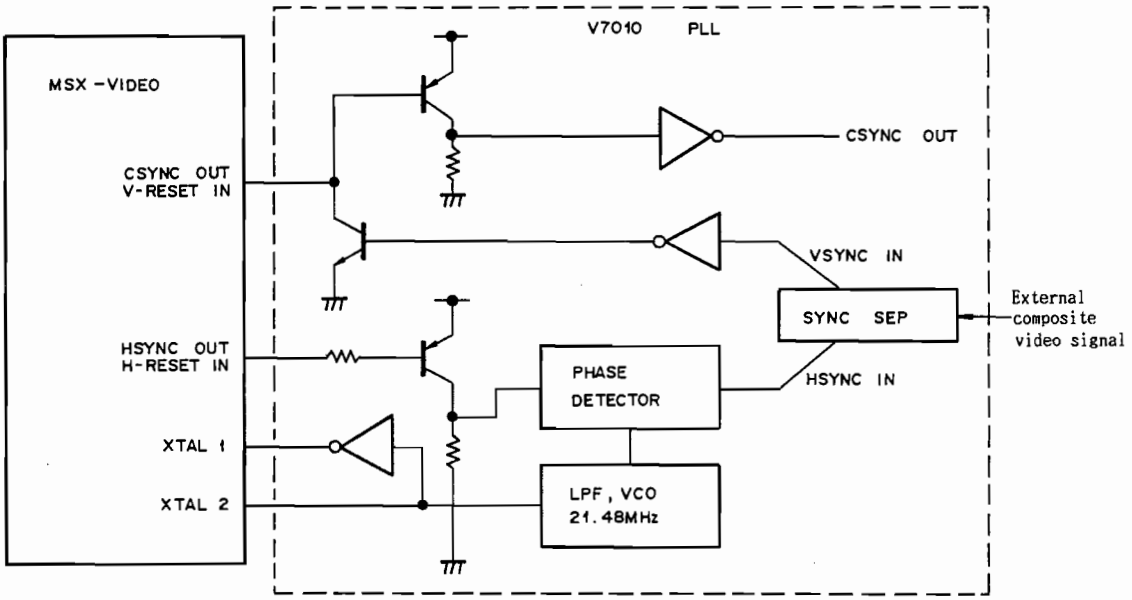


Fig. 9-15 GENLOCK method

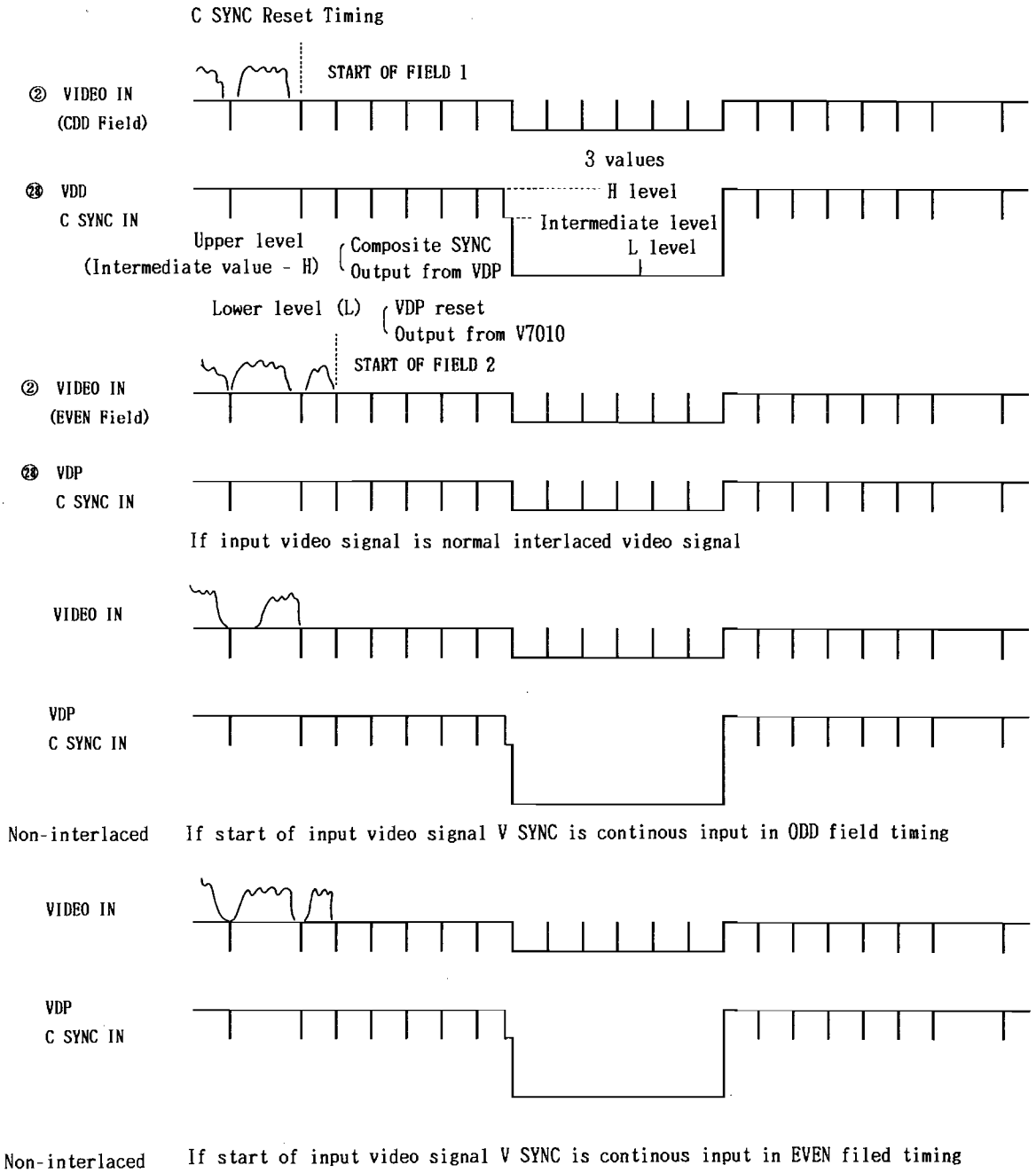
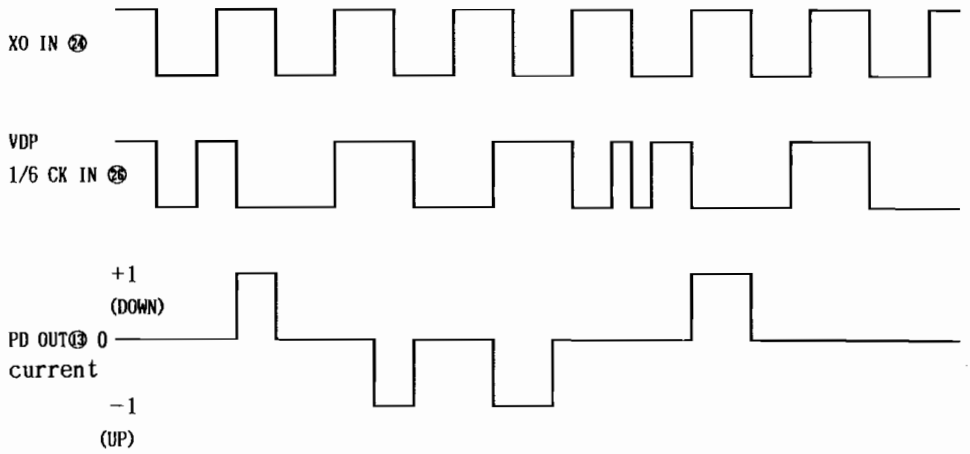


Fig. 9-16 Timing chart (1)

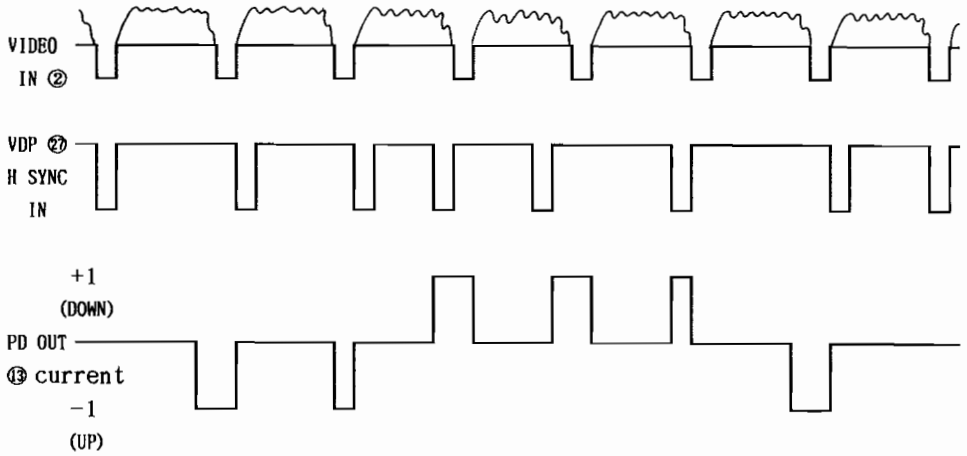
PD OUT output timing chart

○When PC is H



The direction in which current flows into the IC is taken as the positive direction.

○When PC is L



Since the C SYNC separated from the video signal applied to the VIDEO IN pin, and the H SYNC pulse applied to the H SYNC IN pin are passed via a half H killer circuit, a 1/2H pulse is eliminated.

○No output when SW TC is L

Fig. 9-17 Timing chart (2)

9.2.3 Synchronization Mode selection

MSX-VIDEO mode is specified by the two bits S1 and S0 in the R#9 register.

MSB 7 6 5 4 3 2 1 0 LSB

R#9 [S1 S0] Mode register 3

S1	S0	Synchronization modo	$\overline{Ys}$	Purpose
0	0	Personal computer synchronization	MSX-VIDEO always selected (0)	MSX-VIDEO screen display
0	1	Standard synchronization	Generated transparent section on display screen	Display of external signals such as superimposed and digitized signals
1	0	Standard synchronization	External signal always selected (1)	
1	1			

Table 9-6

9.2.4 Superimposing

MSX-VIDEO can generate a switching signal ($\overline{Ys}$) used to superimpose external video signals on the MSX-VIDEO output.

- The MSX-VIDEO synchronizing signal must be matched with the signal to be superimposed.
- If an interlaced display picture is used, MSX-VIDEO will also appear as an interlaced display.

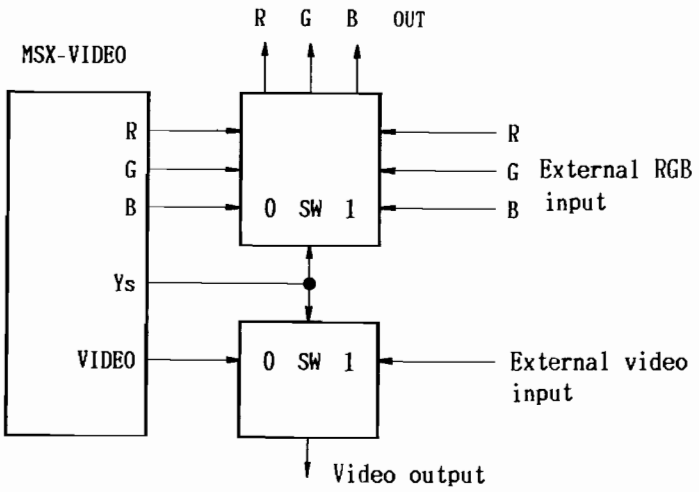


Fig. 9-18 Superimposing

Since $\overline{Ys}$ is changed to high level when MSX-VIDEO scans the transparent section of the screen, the external video signal is selected.

9.2.5 Software Control of AV Switcher

UC-V102 is equipped with an AV switcher which selects the input pin for external input signals when output data is passed directly to the I/O port (50H).

Format OUT &H50, No.
Conditions $0 \leqq No. \leqq 3$
No. : Numerical variable, array variable, expression (No. should not be greater than 3)
No. = 0 : Select RGB multi-connector pin input.
No. = 1 : Select input applied to video/audio input pin 1.
No. = 2 : Select input applied to video/audio input pin 2.
No. = 3 : Select input applied to video/audio input pin 3.

The input applied to video/audio input pin 1 is selected when UC-V102 is reset. Note that external input signals selected by this command can be superimposed with personal computer images and mixed with personal computer sound by the BASIC SET VIDEO command.

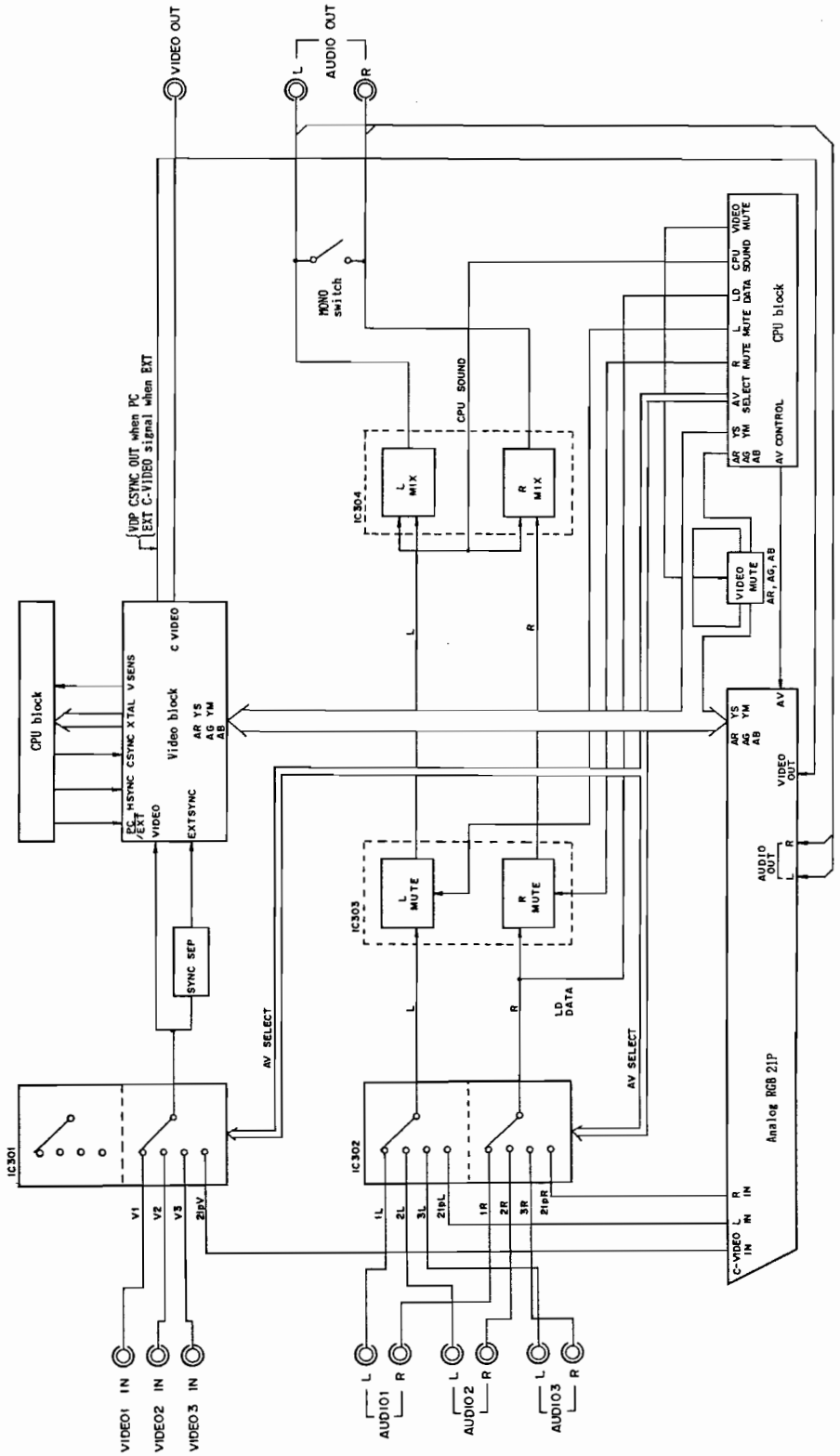
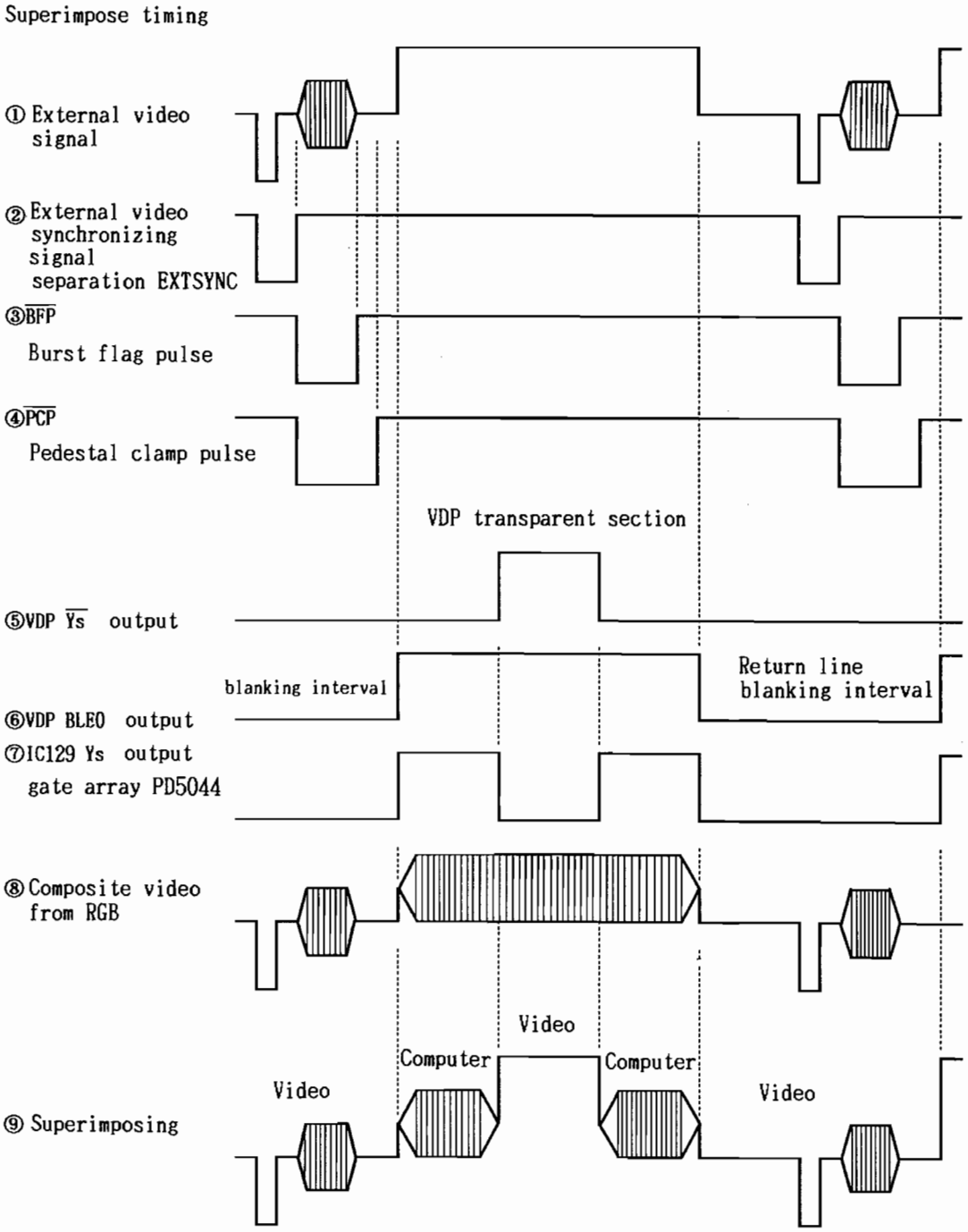


Fig. 9-19 AV switcher block diagram



Note : BASIC SET VIDEO command invalidates video input control.

Fig. 9-20 Superimposing time chart

10. OPTIONAL FLOPPY DISK DRIVE INSTALLATION PROCEDURE

1. Switch the power off and remove the bonnet.

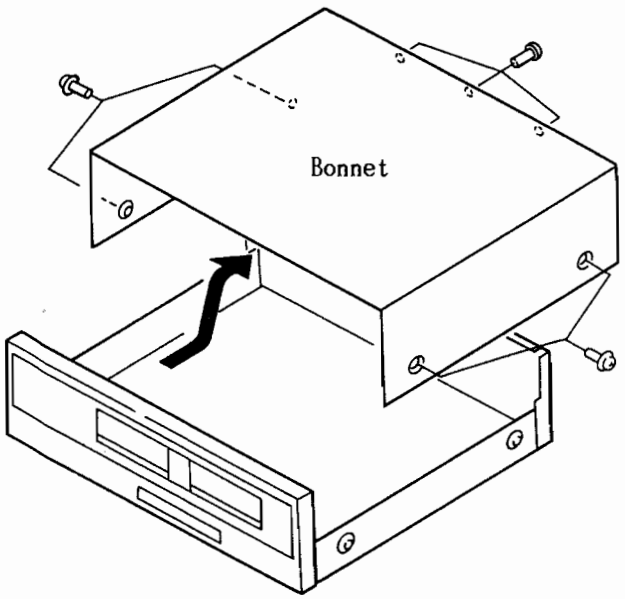


Fig. 10-1

2. Remove the disk cover and FD mounting bracket.

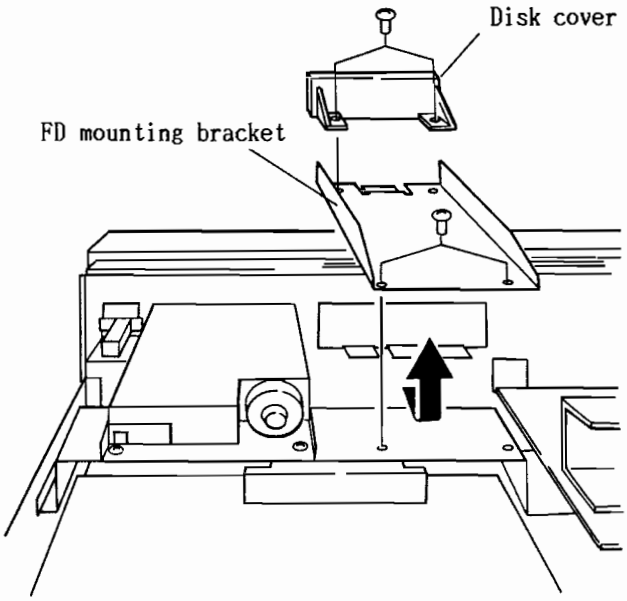


Fig. 10-2

3. Change the shorting socket located in the switch stage (see Figure 10-3) under the floppy disk drive (FDD) from DS0 to DS1.

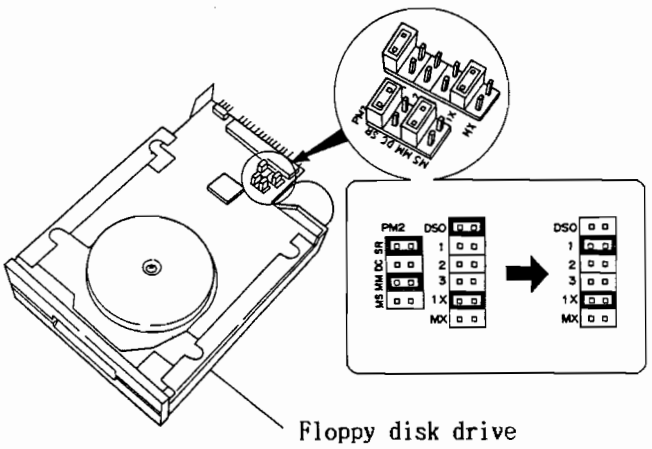


Fig. 10-3

4. Secure the FDD to the FD mounting bracket with the drive well centered in the bracket.

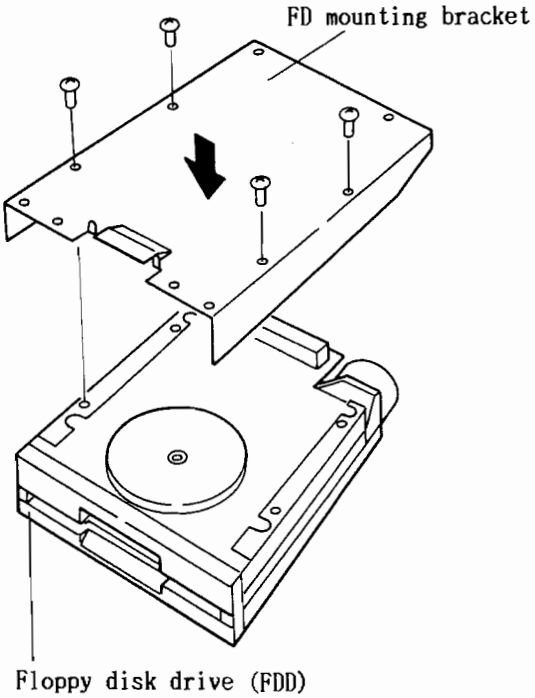
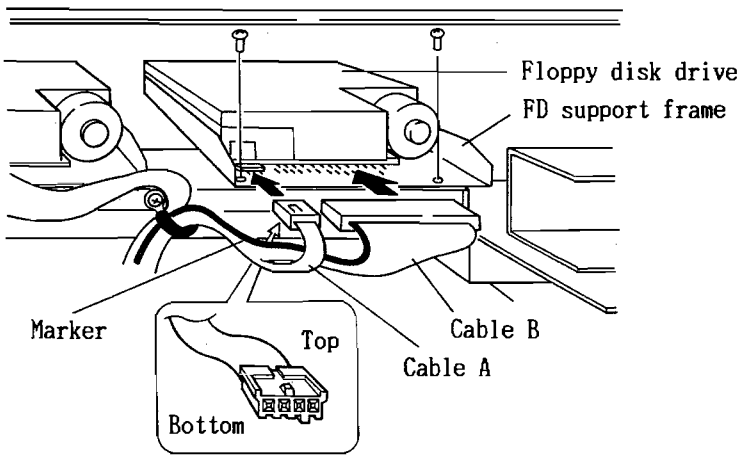


Fig. 10-4

5. Secure the FD mounting bracket (with FDD) to the FD support frame.
6. Then connect cable A to the FDD as shown in Figure 10-5, and connect cable B with the marker side facing as shown in the diagram.



Cross-section of cable A connector

Fig. 10-5

7. Secure the bonnet.
8. Switch the power on.
9. Start BASIC and insert a diskette in drive B. Key in FILES"B:RETURN and check that the diskette contents are correctly displayed.

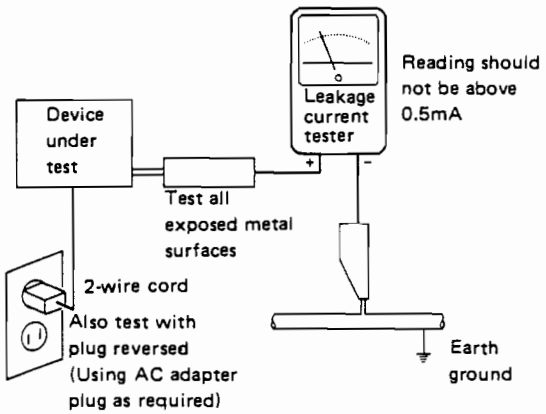
11. SAFETY INFORMATION

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.